240 W CCM Totem-pole PFC with CoolGaN™ IPS and XMC™

REF_240W_TP_PFC_GaN

About this document

Scope and purpose

This document presents a system solution based on Infineon wide-bandgap (CoolGaN™) integrated power stage, superjunction (CoolMOS™) power semiconductors and, drivers and microcontroller for a bridgeless totem-pole power factor corrector (PFC). The REF_240W_TP_PFC_GAN board is intended for applications that require low-power delivery at low-profile (20 mm) and high-power density (87 W/in^3) such as USB PD or battery chargers. The totem-pole implemented in the REF_240W_TP_PFC_GAN board operates in continuous conduction mode (CCM) at 70 kHz switching frequency, with full digital control implementation on Infineon XMC™ 1400 series microcontroller.

The Infineon components used in this 240 W bridgeless totem-pole PFC board are:

- 600 V CoolGaN™ Integrated Power Stage (IPS): Single-package integration of EiceDRIVER™ gate driver and CoolGaN™ GIT HEMT
- 600 V CoolMOS™ P7 superjunction (SJ) MOSFET
- EiceDRIVER™ 2EDB8259E isolated gate drivers
- XMC1402 microcontroller

Intended audience

This document is intended for design engineers of applications such as USB-C or battery chargers, who want to explore the implementation of a CCM totem-pole PFC with 650 V CoolGaN™ and 600 V CoolMOS™ devices in SMD package, along with EiceDRIVER™ and XMC™ microcontroller.

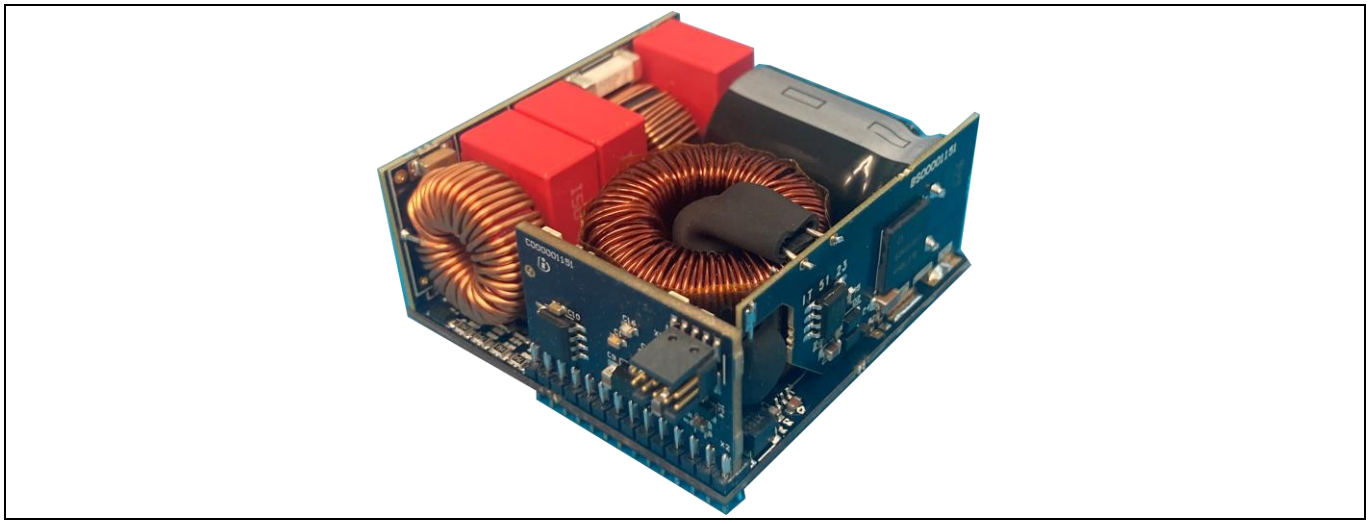


Figure 1 REF_240W_TP_PFC_GaN

Table of contents

About this document **1**
Table of contents **2**
Important notice **3**
Safety precautions **4**
1 System description **5**
1.1 Board description 7
1.2 Board AC and DC connections 9
2 Board specifications and test results **10**
2.1 Steady-state performance 11
2.1.1 Thermal measurements 12
2.1.2 Steady-state waveforms 13
2.2 Power line disturbance 14
2.2.1 Line cycle drop-out (LCDO) 14
2.2.2 Voltage sag 18
2.3 Output voltage dynamic behavior 20
2.3.1 Dynamic load transient response 20
2.3.1.1 Improved output voltage response: undershoot detection 21
2.3.1.2 Overvoltage protection 22
2.3.2 AC voltage variation 23
2.3.2.1 Average and peak inductor current limitation 23
2.3.2.2 Reverse current protection 24
2.4 EMI measurements 25
3 Design considerations **26**
3.1 CoolGaN™ IPS driving and layout 26
3.2 Operation of CoolGaN™ HEMT using unipolar supply voltage and bootstrap 27
3.3 Variable dead-time for natural ZVS in partial load condition 30
3.4 Cooling system for final form factor and extended power range operation 33
3.5 CrCM-TCM vs CCM EMI 36
3.5.1 Comparison of EMI emissions and required attenuation 36
3.5.2 Differential mode EMI designs for CrCM, TCM, and CCM 38
4 Summary **41**
5 Schematics **42**
6 Bill of materials **45**
References **48**
Authors **48**
Revision history **49**
Disclaimer **50**

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Safety precautions

Note: Please note the following warnings regarding the hazards associated with development systems.

Table 1 Safety precautions

	**Warning:** *The DC link potential of this board is up to 500 VDC. When measuring voltage waveforms by oscilloscope, high voltage differential probes must be used. Failure to do so may result in personal injury or death.*
	**Warning***: The evaluation or reference board contains DC bus capacitors which take time to discharge after removal of the main supply. Before working on the converter, wait five minutes for capacitors to discharge to safe voltage levels. Failure to do so may result in personal injury or death. Darkened display LEDs are not an indication that capacitors have discharged to safe voltage levels.*
	**Warning:** *The evaluation or reference board is connected to the AC input during testing. Hence, high-voltage differential probes must be used when measuring voltage waveforms by oscilloscope. Failure to do so may result in personal injury or death. Darkened display LEDs are not an indication that capacitors have discharged to safe voltage levels.*
	**Warning:** *Remove or disconnect power from the drive before you disconnect or reconnect wires, or perform maintenance work. Wait five minutes after removing power to discharge the bus capacitors. Do not attempt to service the converter until the bus capacitors have discharged to zero. Failure to do so may result in personal injury or death.*
	**Caution:** *The heat sink and device surfaces of the evaluation or reference board may become hot during testing. Hence, necessary precautions are required while handling the board. Failure to comply may cause injury.*
	**Caution:** *Only personnel familiar with the converter, power electronics and associated equipment should plan, install, commission and subsequently service the system. Failure to comply may result in personal injury and/or equipment damage.*
	**Caution:** *The evaluation or reference board contains parts and assemblies sensitive to electrostatic discharge (ESD). Electrostatic control precautions are required when installing, testing, servicing or repairing the assembly. Component damage may result if ESD control procedures are not followed. If you are not familiar with electrostatic control procedures, refer to the applicable ESD protection handbooks and guidelines.*
	**Caution:** *A converter that is incorrectly applied or installed can lead to component damage or reduction in product lifetime. Wiring or application errors such as undersizing the cabling, supplying an incorrect or inadequate AC supply, or excessive ambient temperatures may result in system malfunction.*
	**Caution:** *The evaluation or reference board is shipped with packing materials that need to be removed prior to installation. Failure to remove all packing materials that are unnecessary for system installation may result in overheating or abnormal operating conditions.*

1 System description

The REF_240W_TP_PFC_GAN reference design is a system solution enabled by Infineon GaN Integrated Power Stage (CoolGaN™ IPS) together with CoolMOS™ P7 series SJ MOSFETs, drivers, and a XMC™ microcontroller. The CoolGaN™ IPS implemented in this reference board integrates an EiceDRIVER™ gate driver and a CoolGaN™ GIT HEMT in a single 8 x 8 mm package, which enables a power density close to 90 W/in^3 with an efficiency up to 98.6 percent at high-line. This reference board is suitable for applications such as USB PD or battery chargers.

In general, the totem-pole topology is simple and offers a reduced part count and full utilization of the PFC inductor and switches [1]. For the mid-power range, PFC converters are typically operated in critical conduction mode (CrCM) or mixed mode, in which discontinuous conduction mode (DCM) is utilized to avoid excessive increase of switching frequency at light load. However, the variable switching frequency used in such an approach complicates the input filter design because of the need to comply with electromagnetic compatibility (EMC) standards.

In contrast to these vastly expanded approaches, this board consists of a bridgeless totem-pole PFC operated in continuous conduction mode (CCM), in which the fixed operating frequency (70 kHz) enables a reduction on the EMC filtering effort. This reference design offers an outstanding power density of over 87 W/in^3 with a peak efficiency of 98.6 percent at a 230 Vrms input voltage and nominal output power. At low-line, the efficiency at 120 Vrms exceeds 97 percent from half-load.

Note: Due to production variations and measurement setup, efficiency variations up to ±0.2 percent could occur in respect to the result shown.

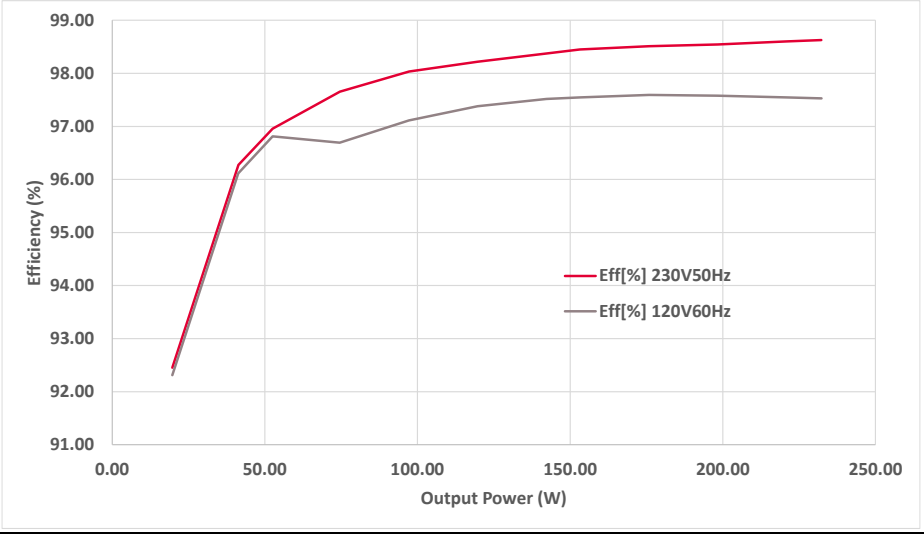


Figure 2 Measured efficiency at 230 Vrms and 120 Vrms of REF_240W_TP_PFC_GAN

The PFC function to achieve bulk voltage regulation while demanding high-quality current from the grid is implemented with an Infineon XMC1404 microcontroller [2]. For more information on PFC control implementation in the XMC™ 1000 family, see the application notes of other Infineon PSU and PFC evaluation boards with classic boost or dual-boost topologies [3], [4], and [5].

The 240 W bridgeless totem-pole reference design presented in this application note is a system solution developed with power semiconductors, drivers, and microcontroller from Infineon as follows:

- 140 mΩ 600 V CoolGaN™ Integrated Power Stage (IGI60F140A1L) in 8 x 8 mm QFN-21 package, as totem-pole PFC high-frequency switches
- 65 mΩ 600 V CoolMOS™ P7 (IPL60R065P7) in ThinPAK 8x8 package for the totem-pole PFC return path (low-frequency bridge) and relay replacement
- EiceDRIVER™ 2EDB8259E isolated gate drivers in TFLGA-13-4 package
- XMC1402 microcontroller in QFN 40-pin package for PFC control implementation

A simplified block diagram of the bridgeless topology with these Infineon devices is shown in Figure 3. The diodes in front of the PFC choke are meant to be a current path for startup or surge conditions; it is not part of the current path during the steady-state converter operation.

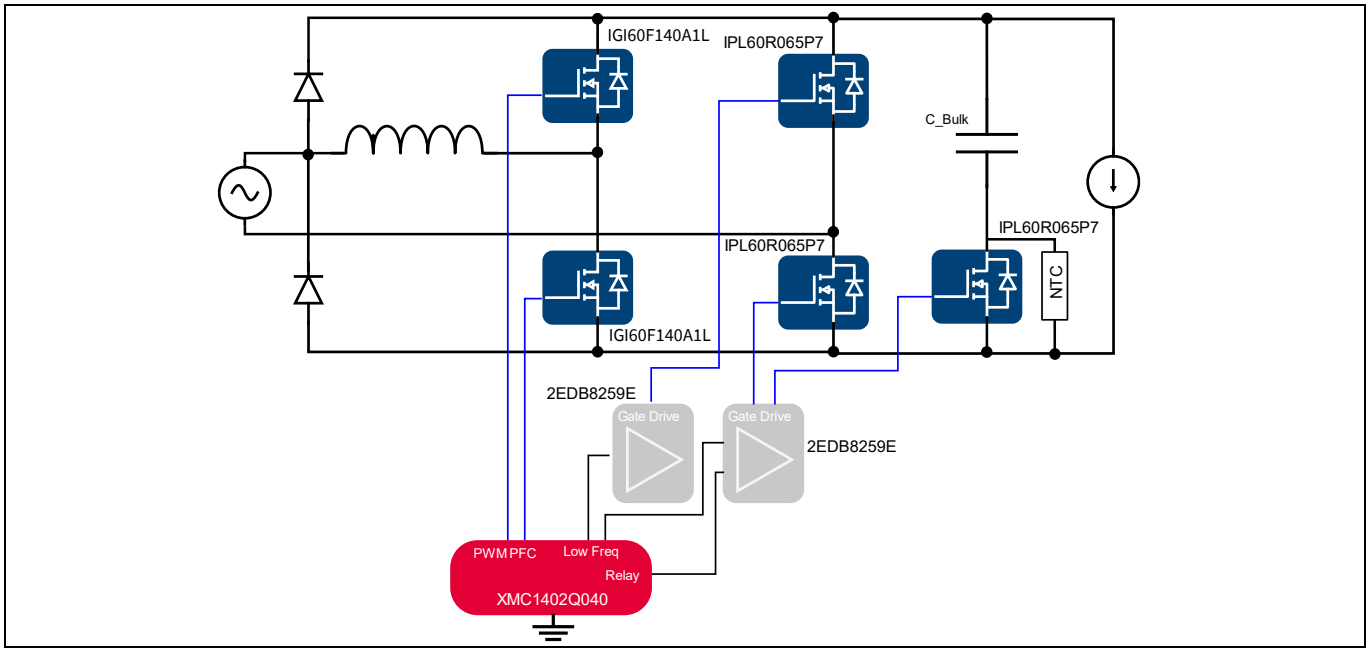


Figure 3 240 W bridgeless totem-pole PFC board (REF_240W_TP_PFC_GAN) simplified diagram showing the topology and Infineon products used

This document describes the REF_240W_TP_PFC_GAN board implementation and provides the specifications and main test results. For further information on Infineon products, visit the Infineon website, the Infineon evaluation board search:

- CoolGaN™ Integrated Power Stage (IPS)
- CoolMOS™ power MOSFET
- Gate driver ICs
- XMC™ microcontrollers

1.1 Board description

Figure 4 shows and overall view of the system presented in this application note and provides an expanded view of the boards that constitute the 240W CCM totem-pole PFC reference design. The board area is 47 mm x 48 mm with a total height of 20 mm, which provides a power density of 87 W/in^3.

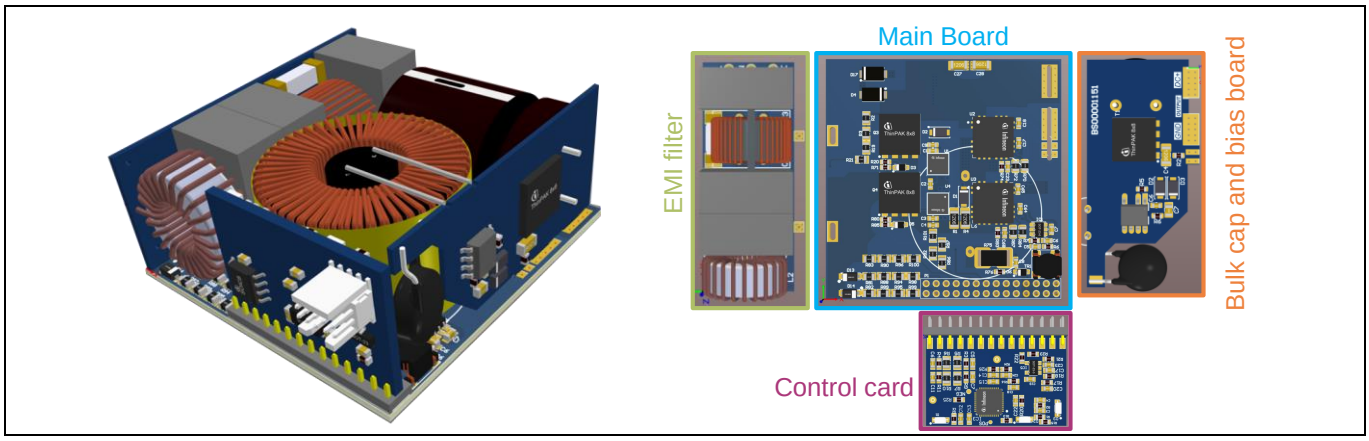


Figure 4 Overall view of REF_240W_TP_PFC_GAN (left) and expanded view of boards that constitute the system (right)

The main board (Figure 5) holds the totem-pole power stage with the CoolGaN™ IPS (orange rectangle) as well as the CoolMOS™ P7 MOSFET and isolated drivers (red rectangle). An isolated charge pump (purple area) is included to supply the control board, since control ground (GND_ISO) is located in the AC line connected to the current shunt resistor (green circle). The PFC choke is implemented with a CH234060GT14 magnetic powder core from Chang Sung Corporation with 105 turns, which is mounted over the power devices in the area marked as a white circle on the PCB.

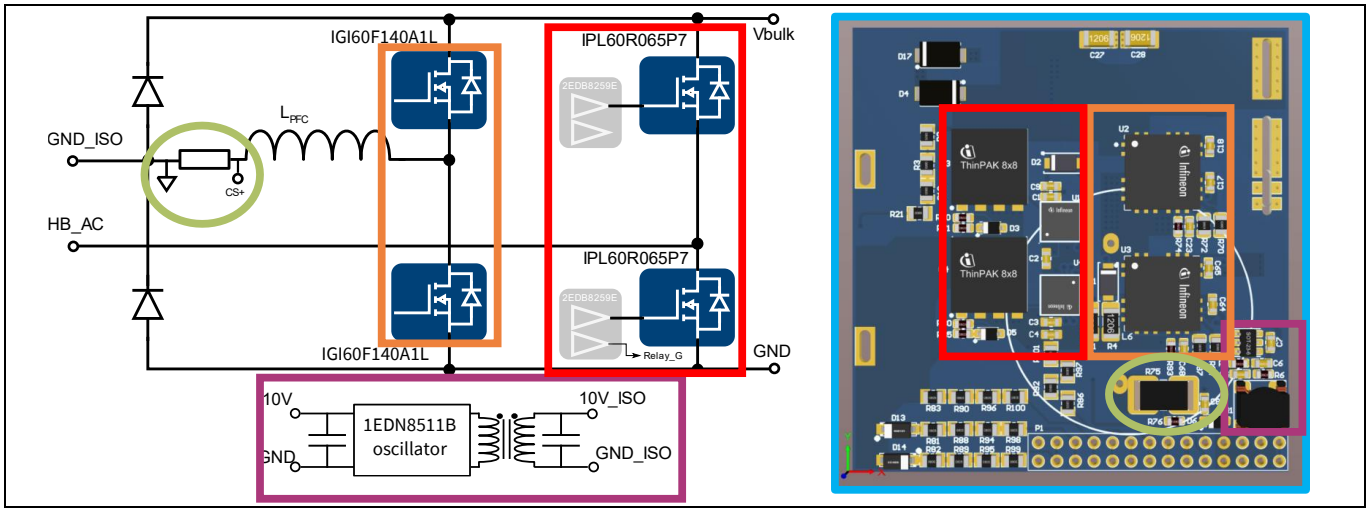


Figure 5 Simplified schematic and main board of REF_240W_TP_PFC_GAN

The EMI filter is mounted vertically and inserted in the main board. As shown in the simplified schematic (Figure 6 – left), the EMI filter is composed of a two-stage filter (from the differential mode perspective):

- One common-mode (CM) choke, in which the stray inductance is used as a differential-mode filter
- One pure differential mode (DM) choke.

This configuration allows to provide enough attenuation in both CM and DM in a reduced form factor as can be seen in the right side of Figure 6.

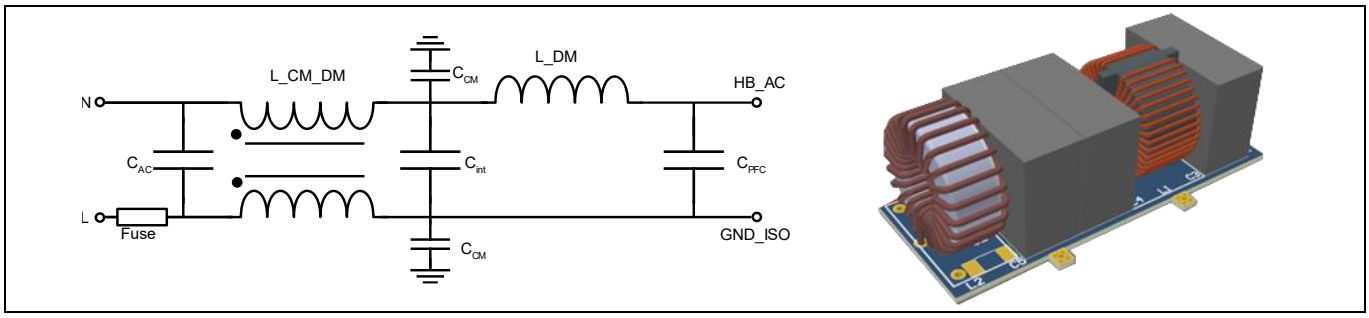


Figure 6 Schematic and 3D view of the EMI filter board

A third board is vertically mounted over the main board, and holds the bulk capacitance and bias power supply (Figure 7). The relay replacement to bypass the NTC (implemented with the same CoolMOS™ P7 MOSFET part as the line rectifiers) is included in this board. The inductor required by the bias buck converter is placed in the inner diameter of the toroidal PFC choke, which is mounted over the main board.

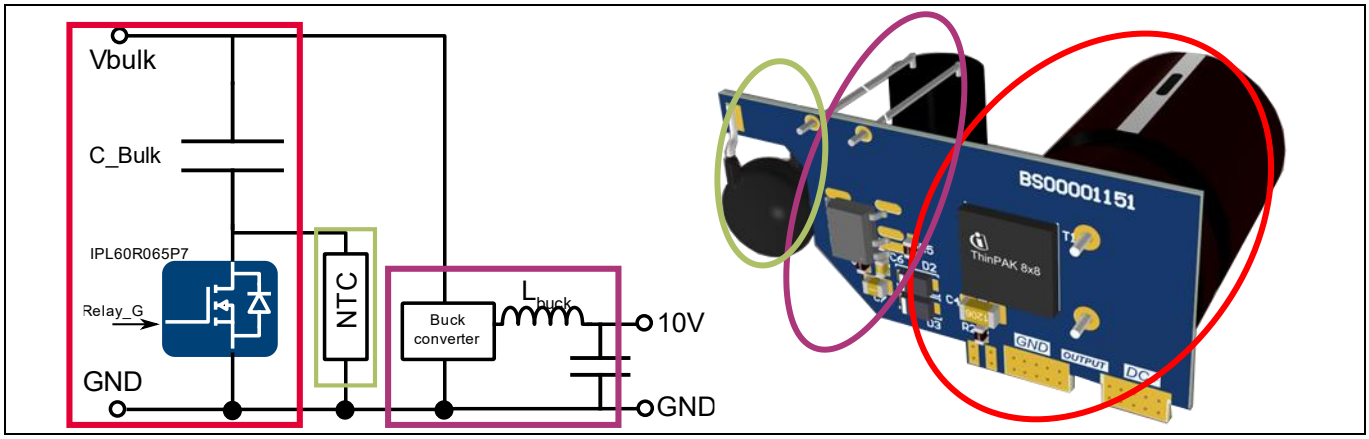


Figure 7 Simplified schematic and 3D view of the bulk and bias board

The control card (Figure 8) mounts the XMC™ microcontroller to implement the PFC function and required sensing circuits. The ground location in REF_240W_TP_PFC_GAN enables the usage of a shunt resistor for current sensing. However, because both positive and negative inductor currents are possible in the bridgeless totem-pole topology, an offset of half of the supply range for the microcontroller is inserted together with the current sense gain to accommodate the ADC input range in the XMC™ microcontroller. The AC is rectified to maximize the ADC range input of the microcontroller; an AC polarity signal is derived taking advantage of the ESD protection of the XMC™ pins and the controller grounding in the AC rail. Finally, the DC sensing requires a differential measurement due to the control ground location. The signal conditioning is explained in more detail in [5].

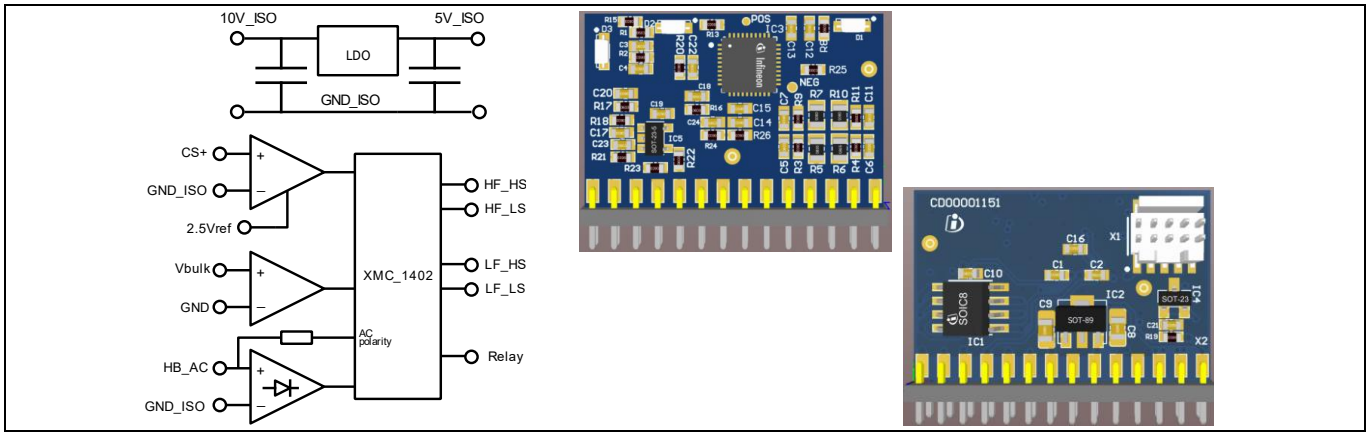


Figure 8 Simplified schematic and top and bottom view of the control card with XMC™ microcontroller

1.2 Board AC and DC connections

The AC and DC connections for REF_240W_TP_PFC_GAN board are shown in Figure 9. Line and neutral connections are available in the EMI filter board. Also, a power earth (PE) connection is provided in case a chassis or earth connection is required (yellow arrow). In the case of DC connections, cables can be directly soldered into the soldering paths of the bias board as shown in the Figure 9.

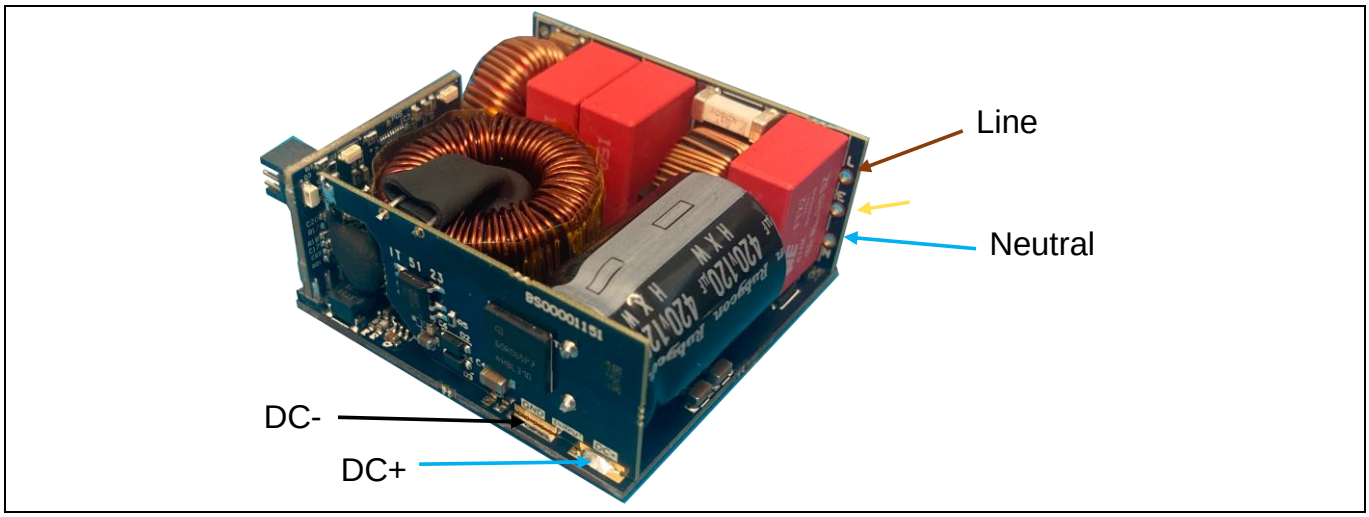


Figure 9 AC and DC board connections available in REF_240W_TP_PFC_GAN

2 Board specifications and test results

This chapter introduces the specifications, performance, and experimental results of the 240 W bridgeless totem-pole PFC in CCM reference design presented in this document. The results presented have been obtained with 140 mΩ CoolGaN™ IPS and 65 mΩ CoolMOS™ P7 MOSFET as low-frequency switches. Table 2 shows the performance and specifications of REF_240W_TP_PFC_GAN under several steady-state and dynamic conditions. The converter operates at 70 kHz switching frequency for universal AC input (90 V – 265 Vrms voltage range) with a 400 V DC output.

Table 2 Specifications and test conditions for the 240 W CCM totem-pole PFC board

Test		Conditions	Specifications	
Efficiency test		90 Vrms, 60 Hz/230 Vrms, 50 Hz	η > 98.5% at 230 Vrms, 240 W η > 96% at 90 Vrms, 240 W	
Current THD		230 Vrms, 50 Hz	THDi less than 10% from 25% load	
Power factor		230 Vrms, 50 Hz	PF higher than 0.9% from 25% load	
Rated DC voltage		–	400 V	
Rated output power		90 Vrms – 265 Vrms, 50 Hz/60 Hz	240 W	
Steady-state Vout ripple		230 Vrms, 50 Hz, 100% load	$\lvert\Delta V_{out}\rvert$ less than 20 $V_{pk\text{-}pk}$	
Power line disturbance	Hold-up time	230 Vrms, 50 Hz or 100 Vrms, 60 Hz; 10 ms AC lost at 100% load	Vout_min = 315 V (UVP)	No damage: • PFC soft start if UVP reached • PFC soft start if AC sag longer than specified
	Voltage sag	Different sag conditions at 100% load		
AC voltage brown-out		–	86 Vrms start, 83 Vrms off	
Load transient		0.06 A (10%) ↔ 0.45 A (90%), 0.2 A/µs	Vout_min = 315 V (UVP) Vout_max = 440 V (OVP)	
Overcurrent protection (OCP)		–	Average current limit 5 A	
			Peak current limit 7.5 A	
EMC conducted emission		–	CISPR 22 (EN 55022) Class B	

2.1 Steady-state performance

Figure 10 presents the efficiency variation with load of the CCM 240 W bridgeless totem-pole design at different input voltages. The measurements are taken after a warm-up period of 10 minutes at full load and a 2 minutes operation per acquired point. A WT3000 power analyzer from Yokogawa Test & Measurement Corporation has been used for efficiency measurements. As shown in Table 2, the efficiency at maximum load is 98.6 percent for the nominal input voltage of 230 V and over 96 percent for 90 V. In the case of 90 V operation, the peak efficiency (~97 percent) occurs at half-load operation.

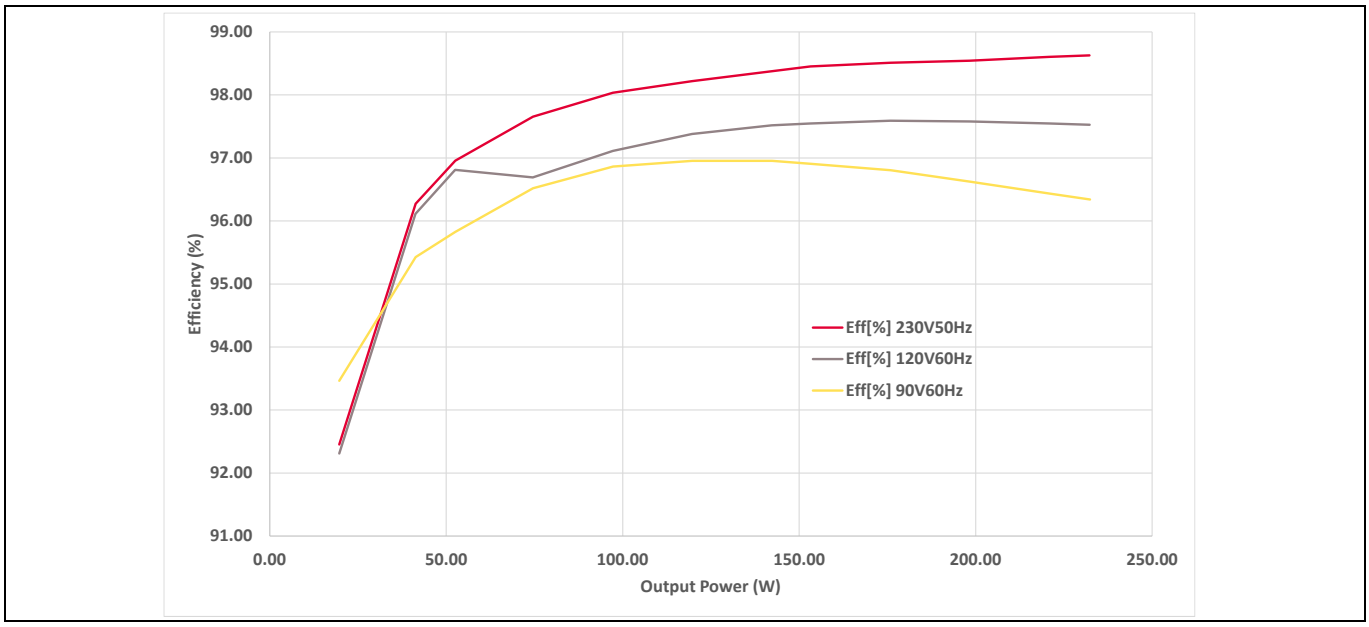


Figure 10 Efficiency variation with the load for REF_240W_TP_PFC_GAN at 230 V 50 Hz, 120 V 60 Hz, and 90V 60 Hz

Regarding the input current performance, the total harmonic distortion (THD) of the input current (Figure 11 – left) is lower than 4 percent for the measured voltages. However, in low-line, the performance is stable with the load while it quickly degrades at light load at nominal input conditions. Nevertheless, the THD remains under 10 percent for loads higher than 25 percent of the nominal output power (approximately 60 W). The power factor (Figure 11 – right) is close to unity for nominal output power and higher than 0.9 for 230 V AC input when the load is higher than 25 percent of the nominal output power.

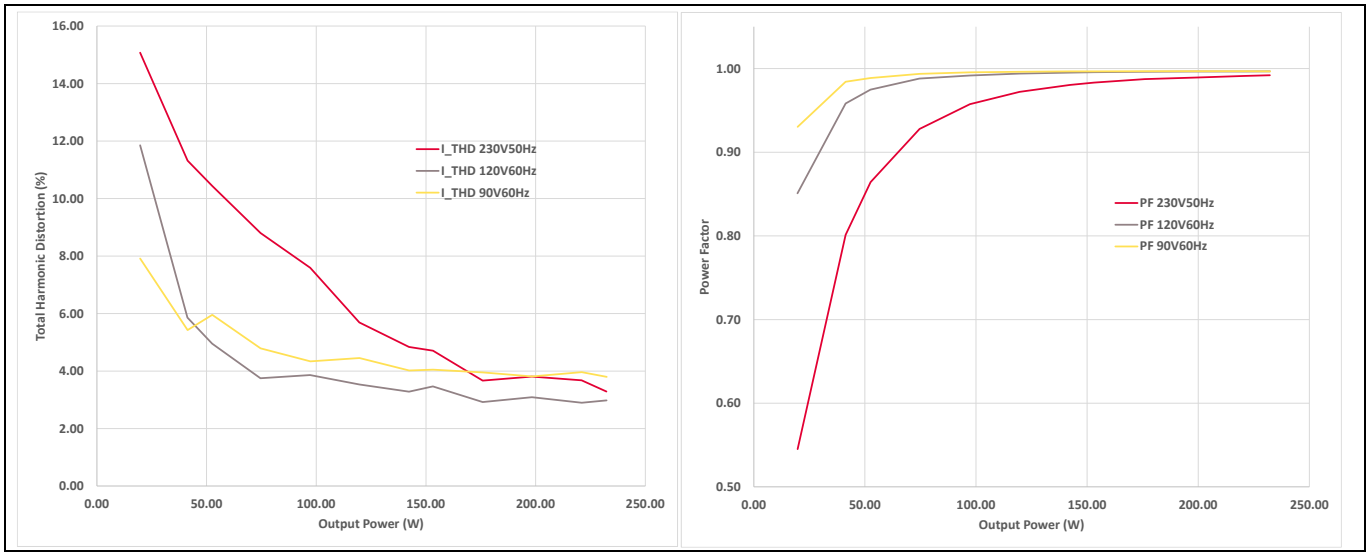


Figure 11 **THD (left) and power factor (right) measurements for REF_240W_TP_PFC_GAN at 230 V 50 Hz, 120 V 60 Hz, and 90 V 60 Hz**

2.1.1 Thermal measurements

For the efficiency test, a thermal capture of the converter after the 10-minute warm-up period at full load is presented in Figure 12.On the left, the thermal behavior of REF_240W_TP_PFC_GAN for 230 V input is shown, while the right introduces the thermal performance for 90 V AC input. In both cases, the CoolGaN™ IPS switches form the hot spot. Special attention must be taken at low-line conditions due to the much higher current flowing through the transistors, PFC choke, and EMI filter. This increased current is reflected in the higher temperatures shown in the thermal capture. To have access to the CoolGaN™ IPS half-bridge for thermal captures, the PFC choke is mounted outside the main board for this test.

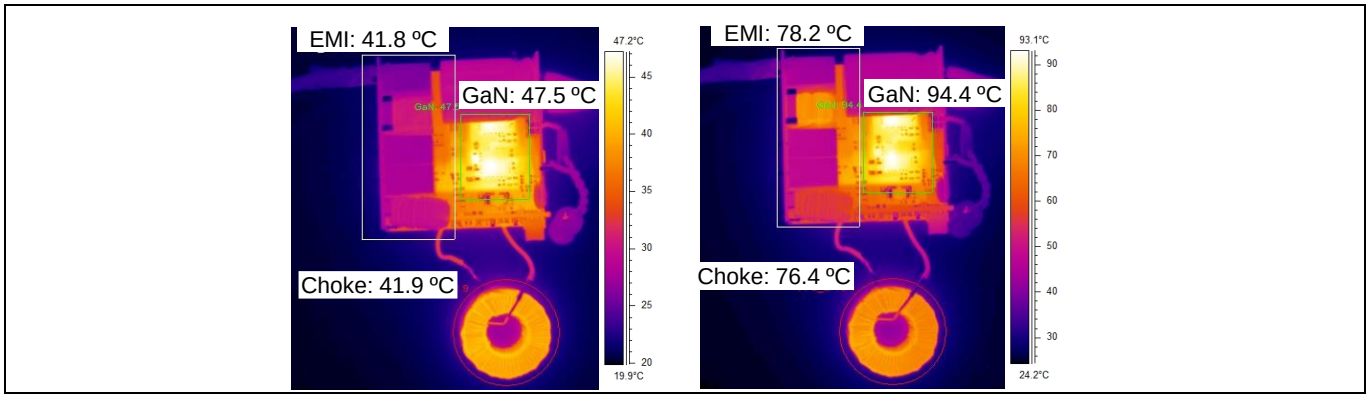


Figure 12 **Thermal captures after 10 minutes of full load operation for 230 Vrms (left) and 90 Vrms (right)**

2.1.2 Steady-state waveforms

The inductor current and input voltage, together with the bulk voltage for 230 V input and nominal output power, are shown in Figure 13. To measure the bulk voltage ripple in steady-state operation (purple waveform), the scope channel has a 300 V offset. The peak-to-peak value of the 100 Hz oscillation in the bulk voltage is 18 V corresponding to a 120 µF ± 20 percent capacitance for 400 V DC output and 240 W nominal output power.

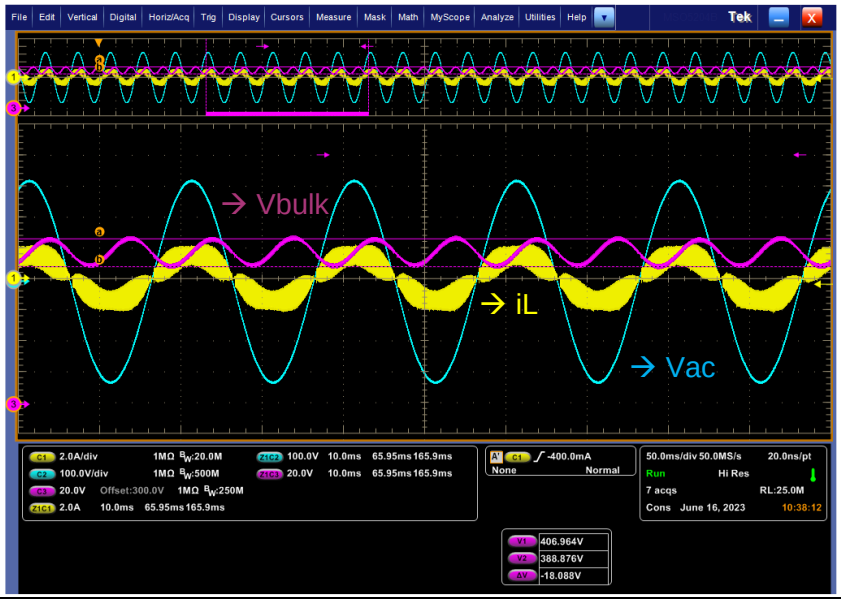


Figure 13 Steady-state bulk voltage ripple for 230 V full-load (0.6A) operation

Figure 14 presents the details of switching cycle waveforms for 100 V 60 Hz operation at 200 W output power (0.5 A load).

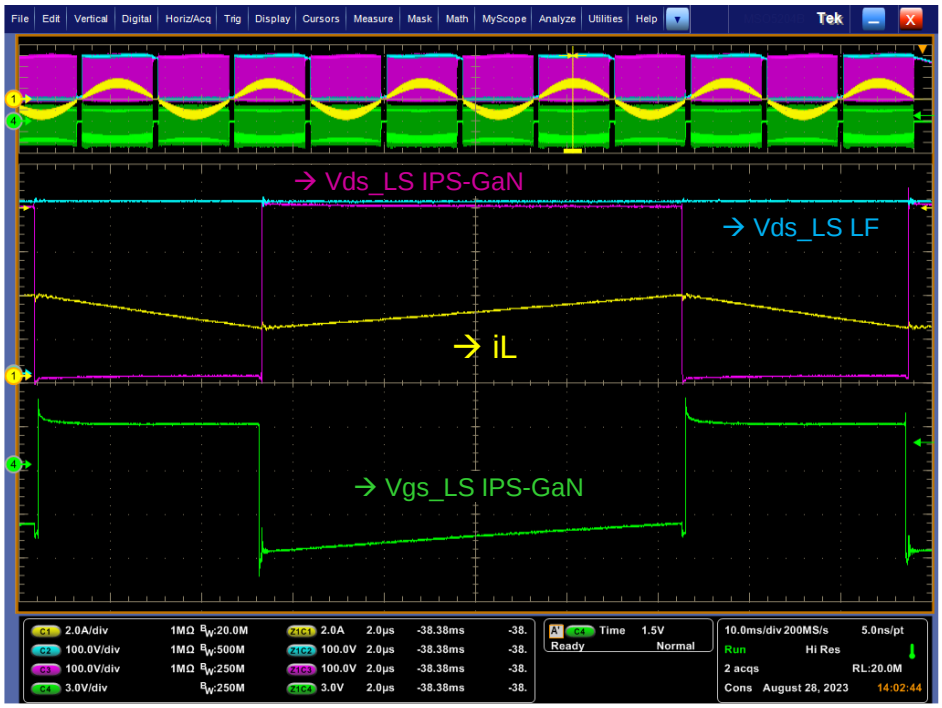


Figure 14 Low-frequency half-bridge switching node: Inductor current and drain-source and gate-source voltage of the CCM totem-pole operating at 100 V 60 Hz AC input and 200 W

2.2 Power line disturbance

Two main abnormal conditions can occur when connected to the grid. On the one side, the AC can be lost during a certain time – line cycle drop-out (LCDO) – and, on the other side, the AC voltage can suddenly decrease to an abnormal value for a period of time – voltage sag.

This section introduces the test conditions for both disturbances as well as the REF_240W_TP_PFC_GAN bridgeless PFC performance when those conditions are applied. For these tests of PFC operation, a programmable AC source and a high-voltage electronic load have been used.

2.2.1 Line cycle drop-out (LCDO)

Because the 240 W design presented in this document can operate at both high-line and low-line, the LCDO capability of the board has been tested in both scenarios according to Table 3 and Table 4. In both cases, a 10 ms maximum hold-up time for nominal output power is considered. The LCDO test has been run starting at different angles and for a repetition of 10 times with a 100 ms period. A 315 V undervoltage protection level (UVP) is programmed in the XMC™ microcontroller and in the electronic load used for the test.

If the UVP threshold is reached due to a longer than 10 ms LCDO for example, the following occur:

1. The totem-pole PFC stops operation.
2. The switch in parallel with the NTC opens.
3. The converter resumes operation with soft-start when the AC and DC voltages are in range.

Table 3 Applied AC cycles for LCDO test at high-line

		1st to 10th time	
Applied voltage	230 V AC (50 Hz)	0 V AC	230 V AC
Timing at different load conditions	100% load	10 ms	90 ms
	50% load	20 ms	80 ms

Figure 15 shows the details of the 230 V test with 10 ms hold-up time. The starting angle of 45 degrees is the worst case from the bulk voltage perspective because when the AC is lost, the bulk voltage is at the minimum value in the 100 Hz oscillation around the steady-state output voltage. To recover faster from the AC lost event, a non-linear control strategy to increase the pumped current to the bulk capacitor is used. More details about that behavior is provided in the output voltage dynamic behavior, see Section 2.3. An example of the 20 ms AC drop-out at half load is presented in Figure 16.



Figure 15 **Detail of the 8th and 9th repetitions of the 10 ms, 45 degrees LCDO test applied at 230 V – 50 Hz and full load**

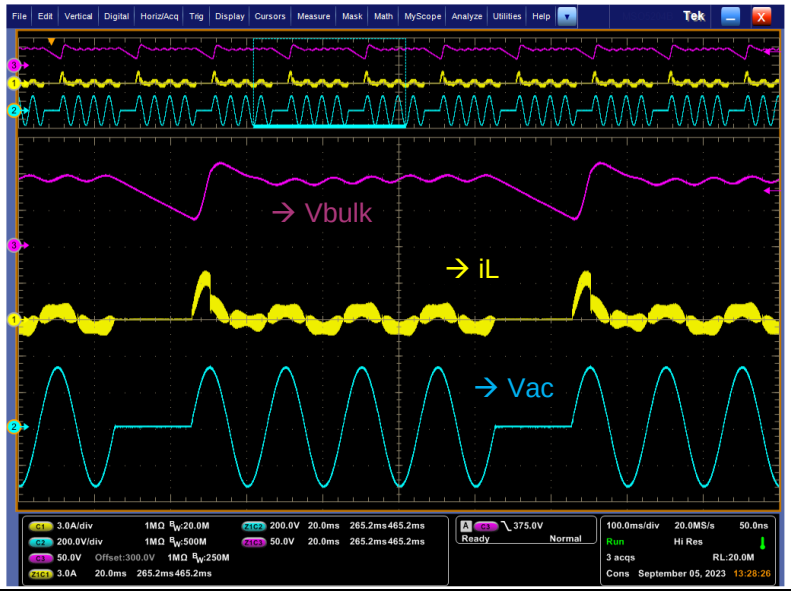


Figure 16 **Detail of the 4th and 5th repetitions of the 20 ms, 0 degrees LCDO test applied at 230 V – 50 Hz and half load**

More details of the switching waveforms for the LCDO at high-line and full load are presented in Figure 17. An explanation on the required sequence to resume the PWM operation after normal and abnormal conditions is presented in Section 3.2.

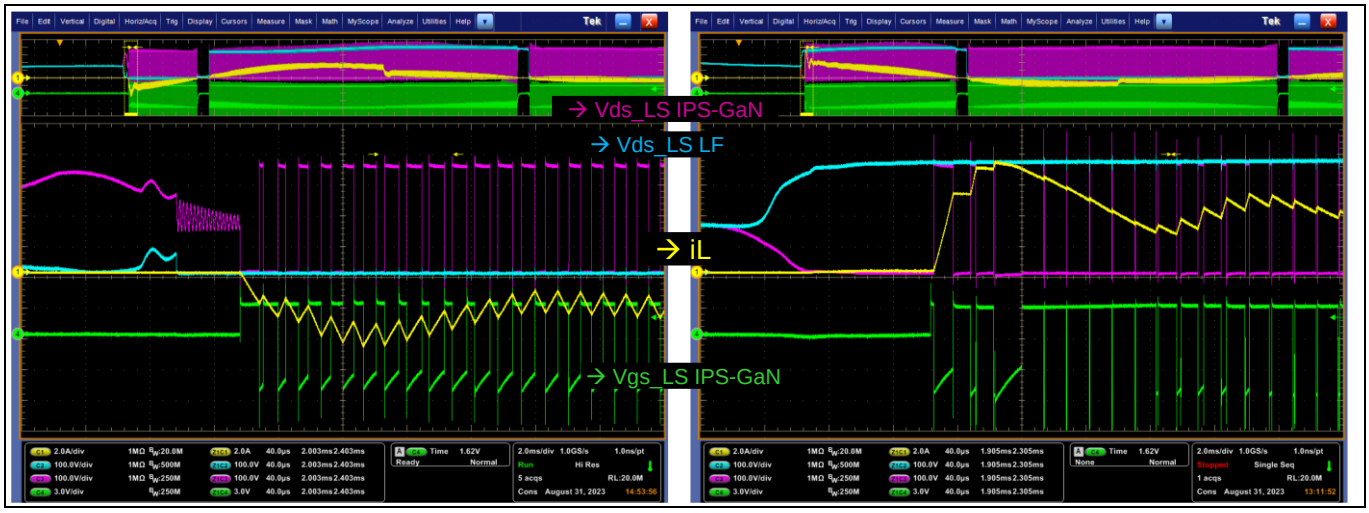


Figure 17 **Switching waveforms for resume of operation after 10 ms LCDO at 230 V and 45 degrees for negative AC voltage (left) and 90 degrees for positive AC voltage (right)**

Table 4 **Applied AC cycles for LCDO test at low-line**

		1st to 10th time	
Applied voltage	100 V AC (50 Hz/60 Hz)	0 V AC	100 V AC
Timing at different load conditions	100% load	10 ms	90 ms
	50% load	20 ms	80 ms

In the case of low-line operation, Figure 18 shows the result for the LCDO test at 100 V and 60 Hz operation when the AC is lost for 10 ms at nominal output power. In this case, due to the increase in current to recover the bulk voltage faster, the maximum average current (set to 5 A) is reached as shown in the presented waveforms.

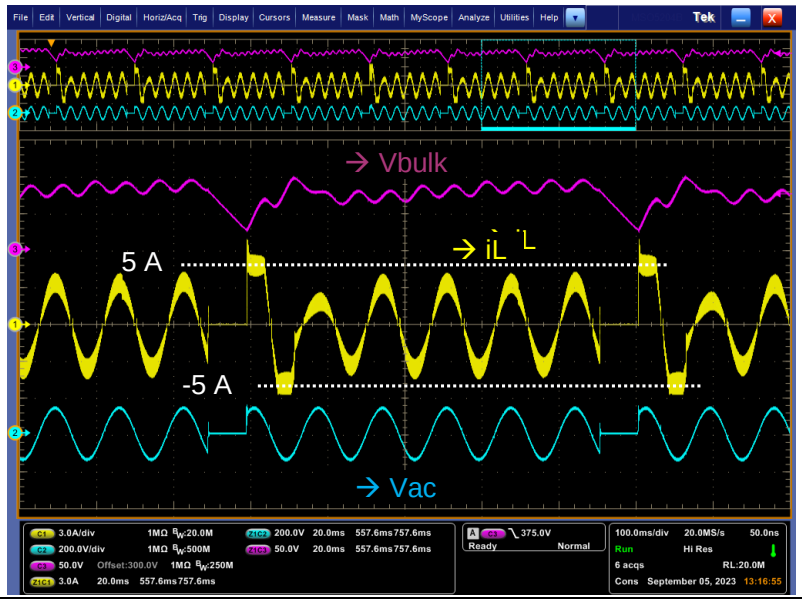


Figure 18 **Details of the 9th and 10th repetitions for the 235 degrees LCDO test applied at 100 V – 60 Hz and full load**

More details of waveforms after a 20 ms LCDO at half load for 100 V and 60 Hz input and different starting angles are shown in Figure 19. The peak and average current limitation is visible in both cases. On the right, due to the very high duty cycle and implementation of the trap function in the controller, some pulses are lost when the peak current limit is reached. Also, the drain-source waveforms are not clamped, which indicate the UVLO of the HS driver (see Section 3.2).

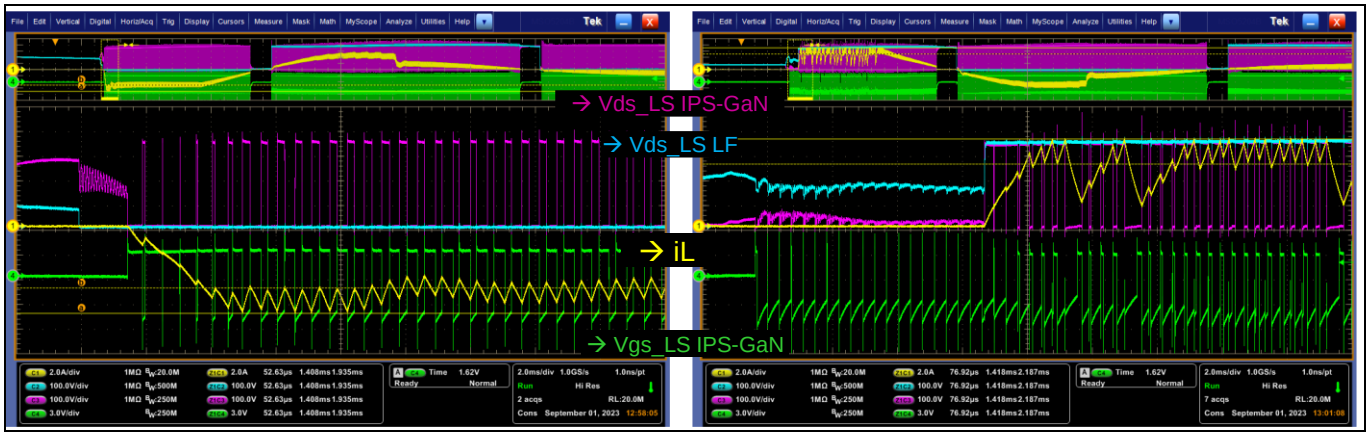


Figure 19 Switching waveforms for resumption of operation after 20 ms LCDO at 100 V – 60 Hz and 0 degrees (left) and 180 degrees (right)

2.2.2 Voltage sag

In the case of high-line (230 V operation), a typical test for voltage sag is 130 V for 500 ms and 150 V for 2 s. Because those voltage levels are within the nominal operating range of REF_240W_TP_PFC_GAN, they will not be considered in this section. Therefore, the presented test in this document is related to the low-line operation as shown in Table 5, taking 100 V as the steady AC input.

Table 5 Voltage sag conditions for high-line applied to REF_240W_TP_PFC_GAN board

		1st to 10th time	
	Steady AC input	Voltage sag (time)	Period
AC input	100 V	75 V (2 s)	20 s
	100 V	68 V (500 ms)	5 s

The test at nominal output power for a voltage sag of 68 V for 500 ms is shown in Figure 20. Due to the sudden change in the AC voltage, which is used to generate the current reference, and the low bandwidth of the voltage loop to guarantee a good steady-state performance, the bulk voltage is distorted. Nevertheless, the converter is able to regulate the voltage during the voltage sag and after the nominal AC voltage (100 V) is recovered.

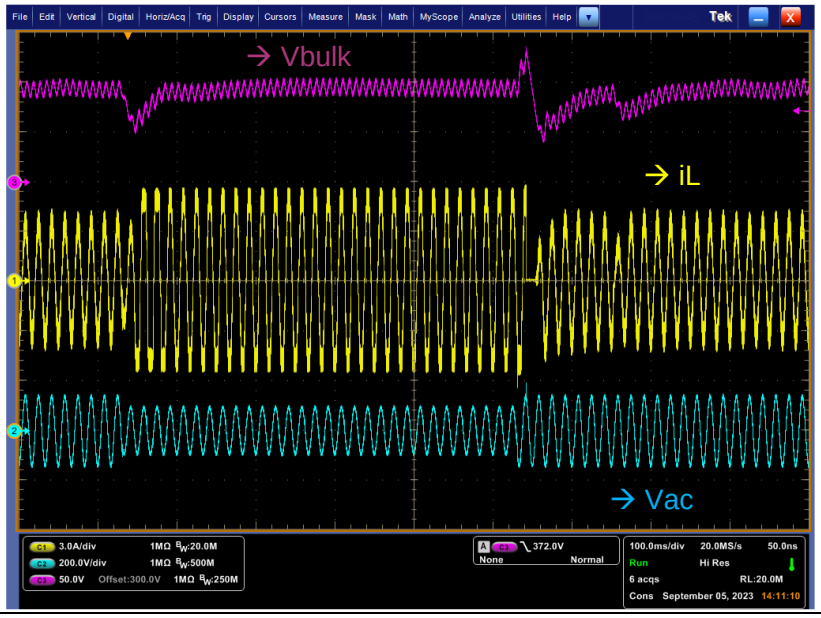


Figure 20 Main waveforms for a voltage sag of 68 V during 500 ms

In the detailed waveforms shown in Figure 21, the output voltage drops when the AC voltage sag occurs due to the sudden reduction of the current reference (left). After a short time, due to the increased current pumped to the bulk capacitor, the voltage is again regulated. The average current limitation to 5 A is also visible in the waveforms. On the contrary, when the 100 V input returns (right side), the sudden increase in current reference provokes an overvoltage detection (OVP) event and the PWM is turned off until the bulk reaches down the target voltage. More details on these non-linear effects will be provided in the output voltage dynamic behavior Section 2.3. The 75 V voltage sag during the two seconds is shown in Figure 22, with a similar behavior of the output voltage.

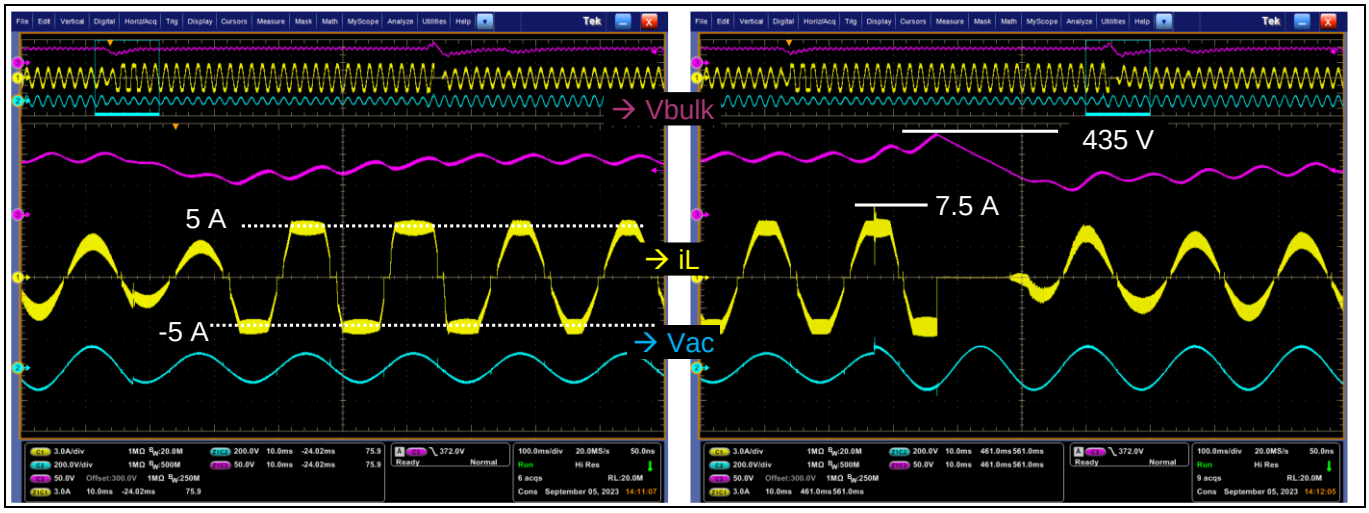


Figure 21 **Details of the main waveforms for the change from 100 V to 68 V (left) and vice versa (right) during the 68 V – 500 ms voltage sag**

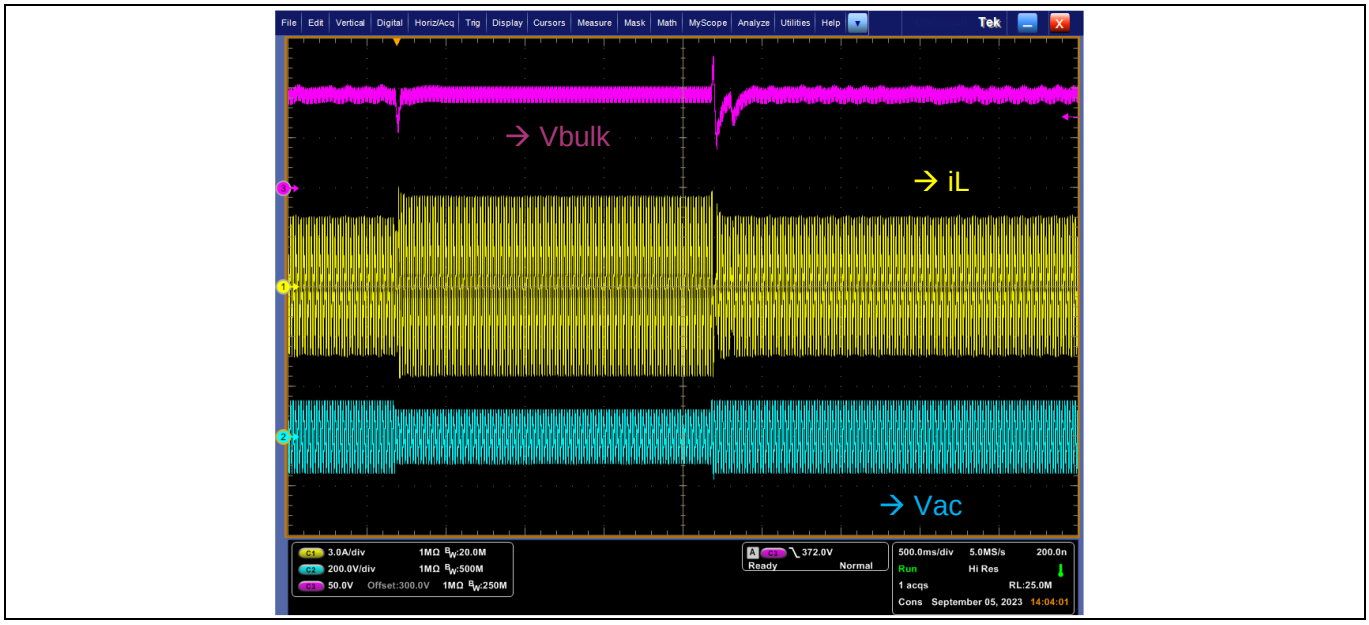


Figure 22 **Main waveforms for a voltage sag of 75 V during 2 s**

In both cases, if the voltage sag lasts longer than the defined time (see Table 5), the converter stops operation, the relay replacement switch opens, and a soft start occurs when the AC and DC voltages are in range. That is the case presented in Figure 23, where a 75 V voltage sag is applied during a 10 percent longer time (2.2 seconds) than the specified time in the Table 5.

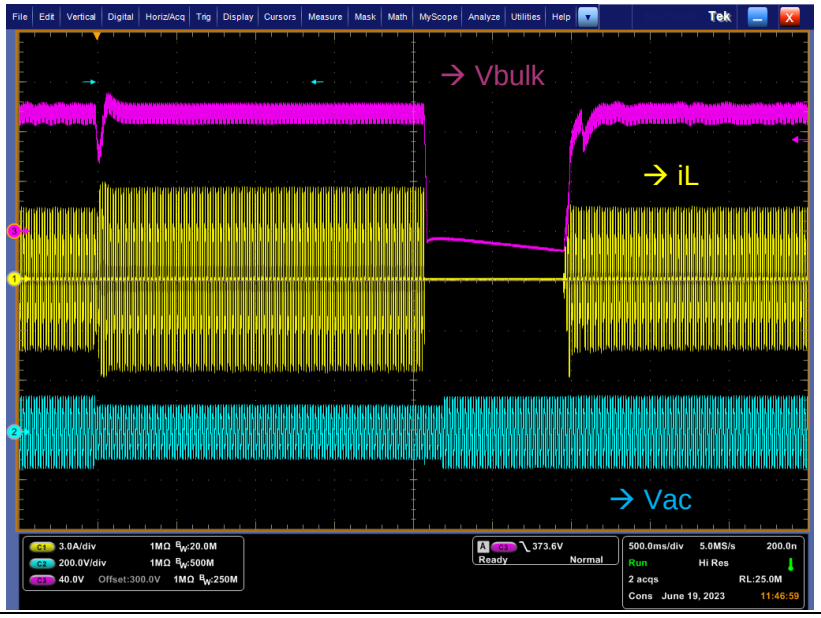


Figure 23 PFC resumes operation after 75 Vrms voltage sag applied for 2.2 seconds at full load

2.3 Output voltage dynamic behavior

The previous section covered the converter response under abnormal conditions related to the AC voltage lost or sag for a certain amount of time. In this section, the focus is the behavior of the REF_240W_TP_PFC_GAN board when the load and the AC voltage are changing inside the nominal range (see the specifications in Table 2).

2.3.1 Dynamic load transient response

The output voltage response of the 240 W CCM totem-pole PFC reference design has been tested for dynamic loading. Figure 24 presents the test result when applying load steps from 10 percent load (0.06 A) to 90 percent load (0.45 A), and vice versa, with 1 A/µs and different timing. On the left, the steps are applied every 200 ms for the 230 V input, while 100 ms steps are applied on the 120 V test reflected in the right. It can be noted that different behaviors happen depending on the bulk voltage. These non-linear response in the output voltage has already been introduced during the abnormal condition tests in the previous section; it will be explained in more detail in the following sections.

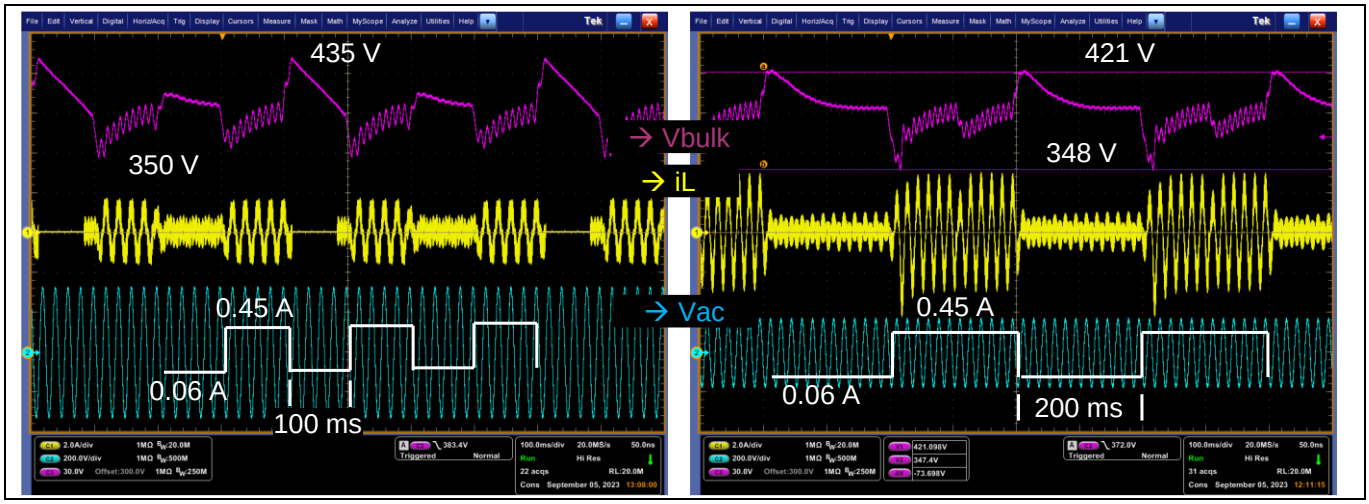


Figure 24 **Bulk voltage response to 10 percent (0.06 A) - 90 percent (0.45 A) load steps, 230 V and 100 ms (left) and 120 V and 200 ms (right) at 1 A/µs**

2.3.1.1 Improved output voltage response: undershoot detection

To provide an excellent input current performance and THD under 5 percent for high-line operation, REF_240W_TP_PF_SIC implements average current control with duty cycle feedforward and the voltage control loop is tuned to 10 Hz. However, in the case of dynamic or abnormal conditions, the slow bandwidth of the voltage loop will provoke very high overshoot and undershoot in the bulk voltage. Therefore, non-linear behavior is implemented in control loops to mitigate the output voltage variation outside steady-state conditions.

If an undershoot is detected (bulk voltage under 360 V), two mechanisms are applied (if the soft start of the target reference is completed) to improve the dynamic response:

- The gain of the voltage loop is multiplied by two for 250 ms after the undershoot is detected.
- The current reference is doubled when the undershoot is detected until the bulk voltage reaches the target voltage.

Two different conditions when the undershoot is detected are shown in Figure 25. On the left, the undershoot mechanisms are triggered due to a 10 percent to 50 percent load step, while on the right, the trigger happens during the resume of operation after a too long 75 V voltage sag.

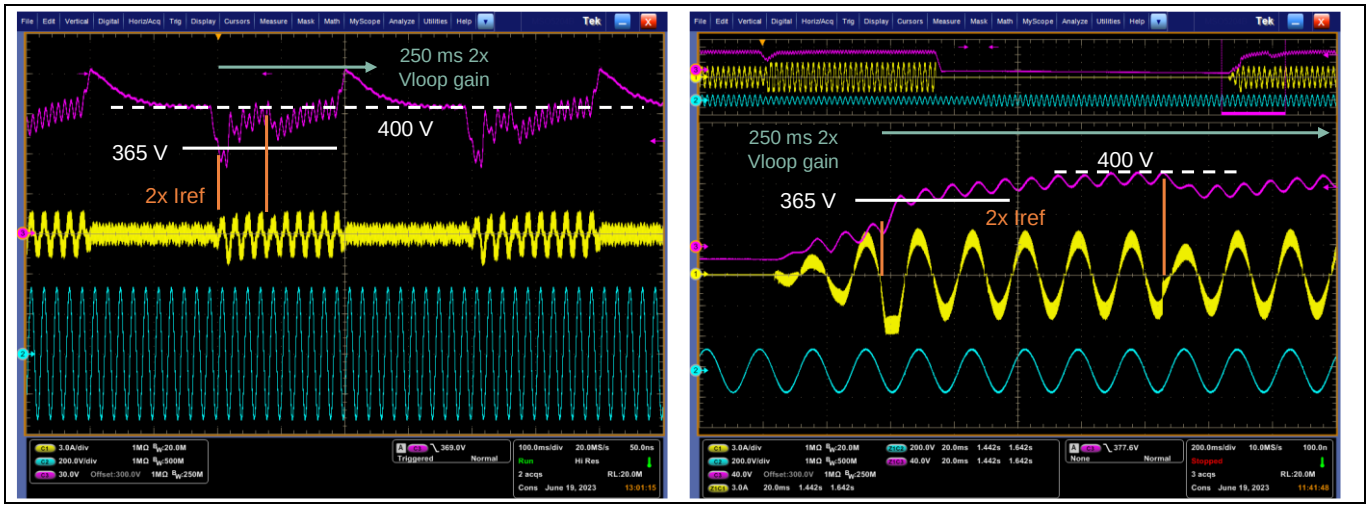


Figure 25 **Increased current and voltage loop gain triggered by undershoot in two different conditions: 10-50 percent load step (left) and start-up at full load (right)**

2.3.1.2 Overvoltage protection

In other conditions such as a load dump or a sudden increase in the AC voltage, the bulk voltage can overshoot. In that case, the PWM is stopped until the voltage decreases to the target value. This behavior is also known as overvoltage protection (OVP). If an overshoot is detected (435 V), the voltage loop is put in hold and reset when the voltage reaches down the target (400 V) and the PWM is resumed at the following AC crossing. In this condition, the low-frequency switches will continue their operation according to the AC voltage polarity to keep the bootstrap capacitor of the high-side driver charged.

Figure 26 shows two conditions in which OVP is triggered. On the left, OVP is triggered due to a load dump, while the right capture presents a sudden change in the AC voltage from 90 V to 230 V. For the latter situation, because the sudden change in voltage that is used to generate the current reference together with the slow reaction of the voltage loop, the current injected into the output capacitor is too large. Therefore, the OVP level is reached, and the operation resumes after the bulk voltage is in the regulation range.

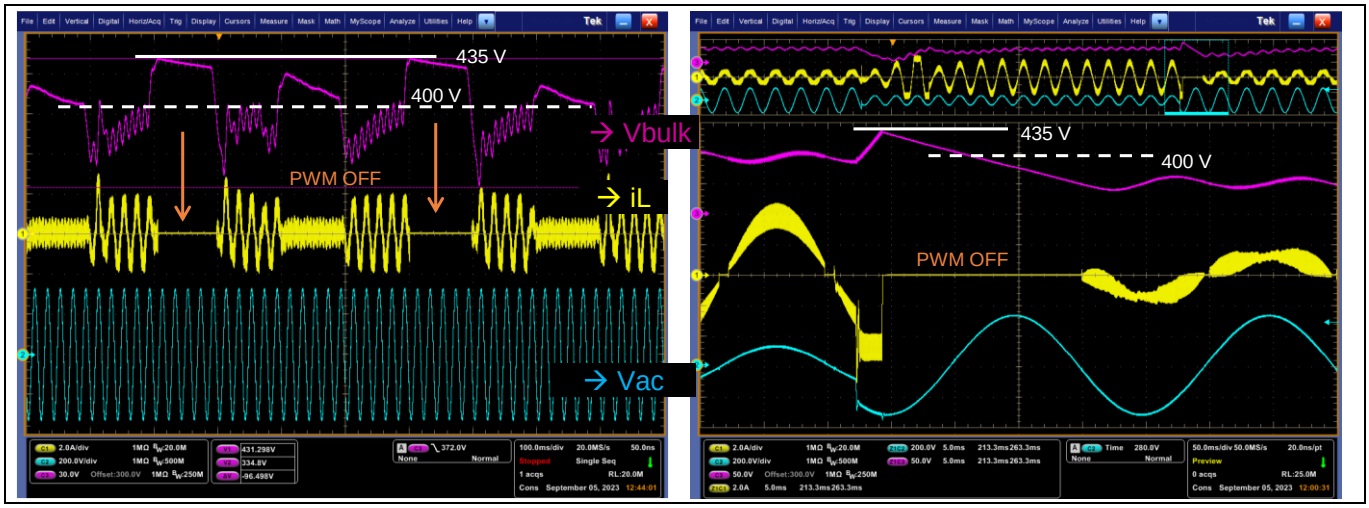


Figure 26 **Trigger of OVP during 0 to 100 percent load variation at 230 V input (left) and after a sudden change of AC voltage from 90 V to 230 V (right)**

2.3.2 AC voltage variation

As can be seen in Section 2.2, changes in the AC voltage significantly influence the output voltage in a PFC converter. This is valid not only for abnormal conditions as already presented but also for AC variations within the specified range.

Figure 27 shows the performance of REF_240W_TP_PFC_GAN under a change in the AC voltage from 230 V and 50 Hz AC input to 90 V and 60 Hz AC input. This reference board control implements a two-stage notch where the first stage is tuned to 100 Hz and the second one is tuned to 120 Hz. Therefore, both 50 Hz and 60 Hz operation are possible without frequency detection and adaptation of notch parameters.

The different non-linear control implementations presented in the previous section are shown in Figure 27. In case of an undershoot, the current reference is temporarily increased as can be seen on the left of the capture when the voltage decreases to 90 V. On the contrary, when the AC returns to 230 V, the sudden changes trigger the OVP, followed by an undershoot detection with an increase in current and voltage loop gain.

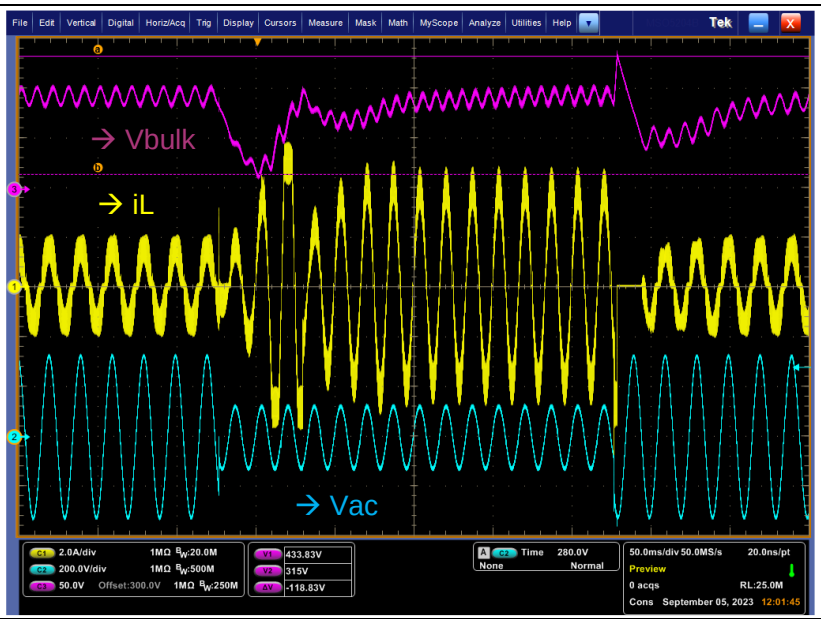


Figure 27 AC voltage variation from 230 V – 50 Hz to 90 V – 60 Hz during 250 ms

2.3.2.1 Average and peak inductor current limitation

Taking a closer look on the waveforms presented in Figure 27, two more protections implemented in the control of REF_240W_TP_PFC_GAN converter can be seen.

Due to the increased current in the case of an undershoot, the maximum current reference is reached as shown in the left of Figure 28. The limitation of current reference implies a limitation of the average inductor current, which is the AC input current. In this board, that current limit is set to ±5 A.

One more level of current limitation is set for those situations in which the average current limitation is not fast enough. The capture in the right of Figure 28 shows the peak current limitation of the inductor current when the AC voltage returns to 230 V from 90 V. This protection is implemented by hardware using the integrated analog comparators connected to the trap function of the XMC™ timers. The peak current is limited to ±7.5 A.

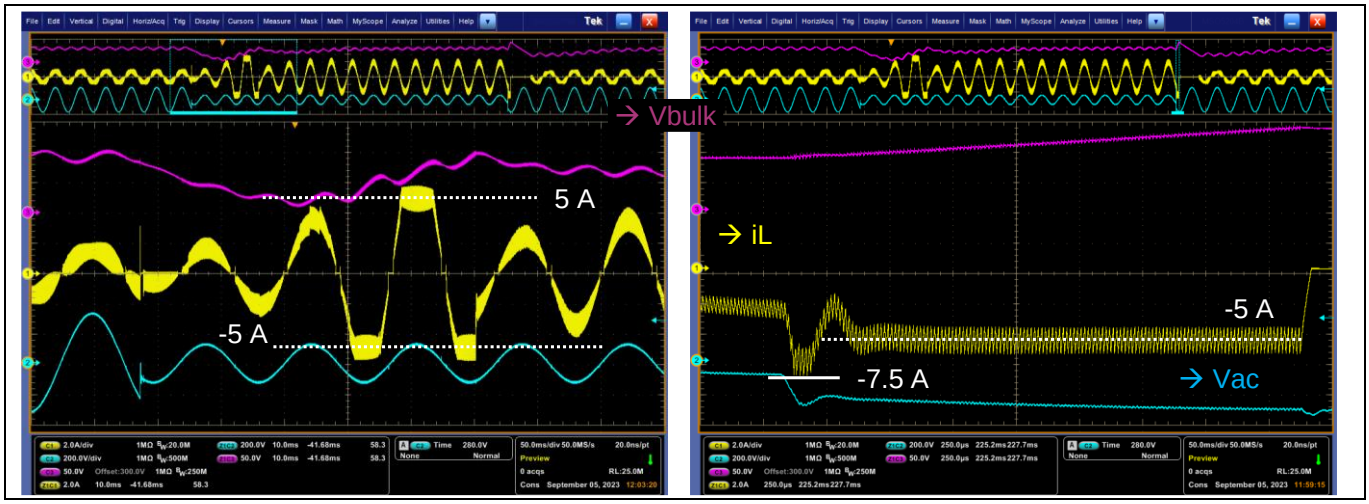


Figure 28 Average (left) and peak (right) inductor current limitations during the AC voltage transient shown in Figure 27

2.3.2.2 Reverse current protection

In the cases where the AC drastically reduces (AC change or LCDO) or if wrong AC polarity is configured after the PWM has been turned off, the average inductor currents may be reversed. Figure 29 shows how the average current changes polarity when a sudden change in the AC voltage occurs. In such a case, the PFC will stop the PWM and resume operation after a defined time (345 µs) as shown in the waveform capture. The average reverse current protection is set to 2 A opposite to the normal current: –2A in the case of Figure 29 because the event happens at a positive AC voltage and therefore causes a positive inductor current. If this condition is detected, the low-frequency switches are both set into passive output. The PFC can continue operation after a defined time (354 µs as shown in the capture) or after the AC crosses zero.

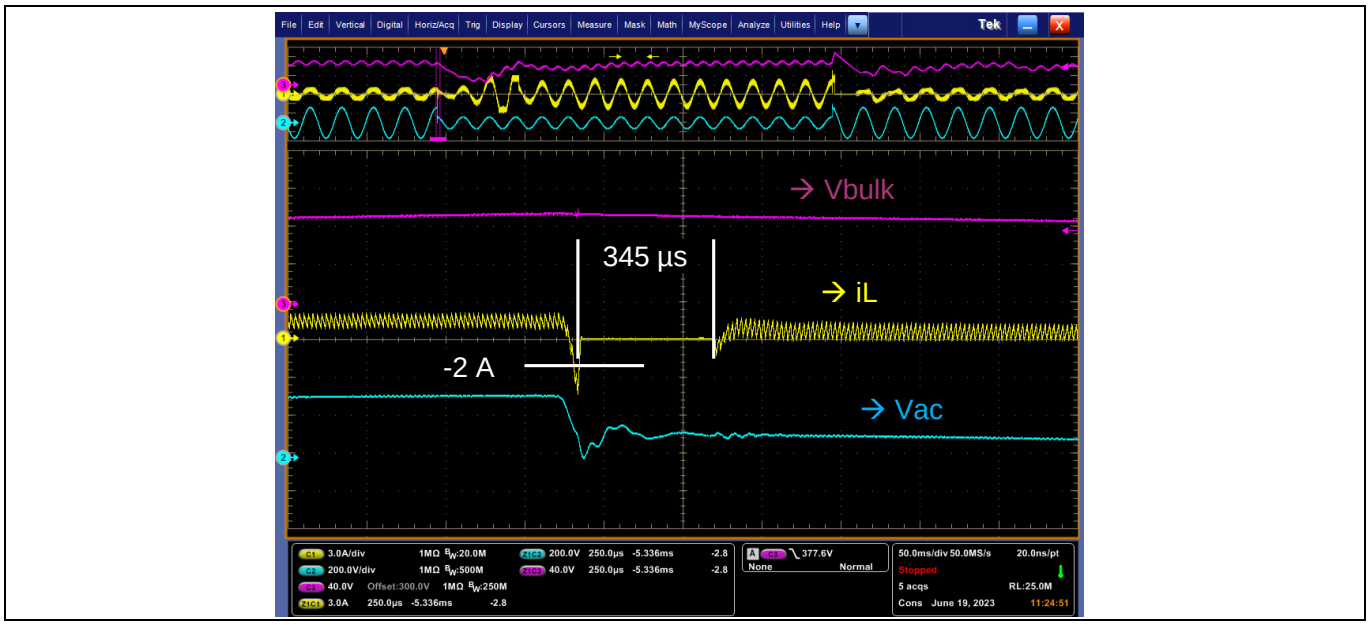


Figure 29 Reverse current due to sudden change in AC voltage

2.4 EMI measurements

The electromagnetic interference (EMI) spectrum has been measured for REF_240W_TP_PFC_GAN using a LISN and resistive load. The results of the conducted EMI measurements run in a non-certified lab are shown in Figure 30. A long margin in the whole spectrum can be observed in respect to the Class B limits for both average and peak measurements. It must be noted that the blue measurement is taken with a peak detector while it is compared to the quasi-peak limits stated in the CISPR 22 standard.

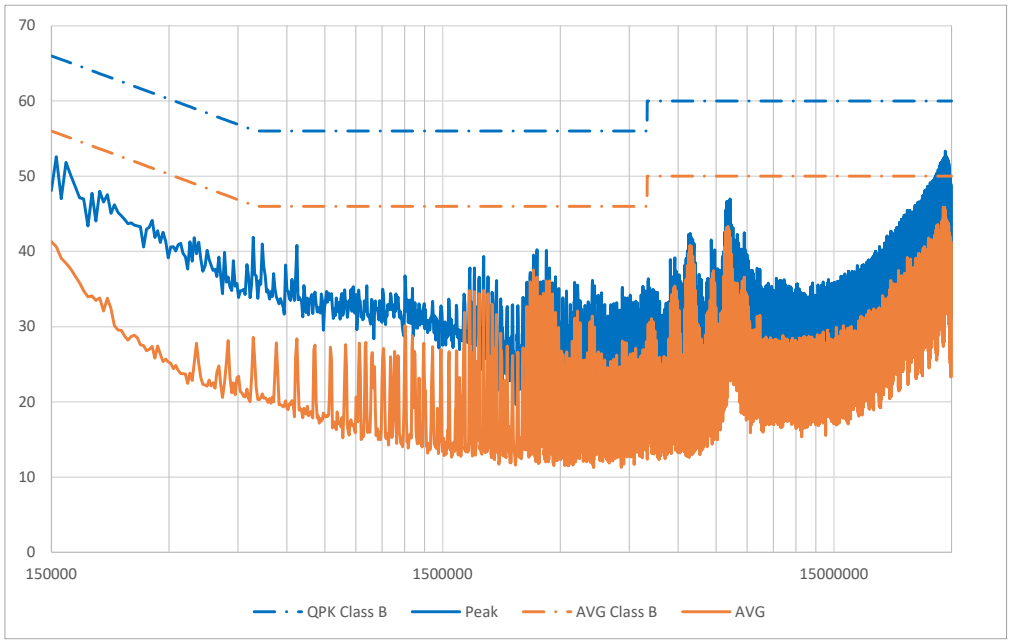


Figure 30 Peak (blue) and average (orange) conducted EMI measurements with resistive load for REF_240W_TP_PFC_GAN

3 Design considerations

The following section introduces the considerations when designing a totem-pole PFC with CoolGaN™ IPS. More details on the design of a totem-pole PFC with CoolGaN™ IPS can be found in [13]:

- Driving and layout of the integrated power stage
- Operation of CoolGaN™ devices with unipolar and bootstrap driver supply
- Capability of ZVS operation in a synchronous boost PFC as implemented in REF_240W_TP_PFC_GAN
- Comparison of differential mode EMI with the most used operating mode in this power level: CCM vs CrCM

Note: It is recommended to use a cooling system (especially for low line AC voltage) due to the highly dense form factor of the presented design and the possibility of operating the board at a higher power at high-line.

3.1 CoolGaN™ IPS driving and layout

The CoolGaN™ integrated power stage (IPS) device used in REF_240W_TP_PFC_GAN integrates an isolated EiceDRIVER™ gate driver together with a 140 mΩ 600 V CoolGaN™ GIT HEMT. Keeping cost as one of the drivers of this reference design, a simple unipolar bias supply with a bootstrap capacitor has been chosen for the control and drivers supply. Therefore, an RC interface of the integrated driver with the CoolGaN™ GIT HEMT is recommended [8]. More information on how to drive the CoolGaN™ HEMT can be obtained in the Infineon CoolGaN™ website, training, and [9].

To minimize the steady-state gate current consumption, the bias supply is set to 10 V and the steady-state gate resistor (Rss in [8]) is set to 10 kΩ. Independent on (2.2 Ω) and off (1.2 Ω) gate resistors are used for optimized fast switching. The coupling capacitor is set to 2.2 nF, which provides fast switching and enables negative bias. The Kelvin source is connected to the source pin.

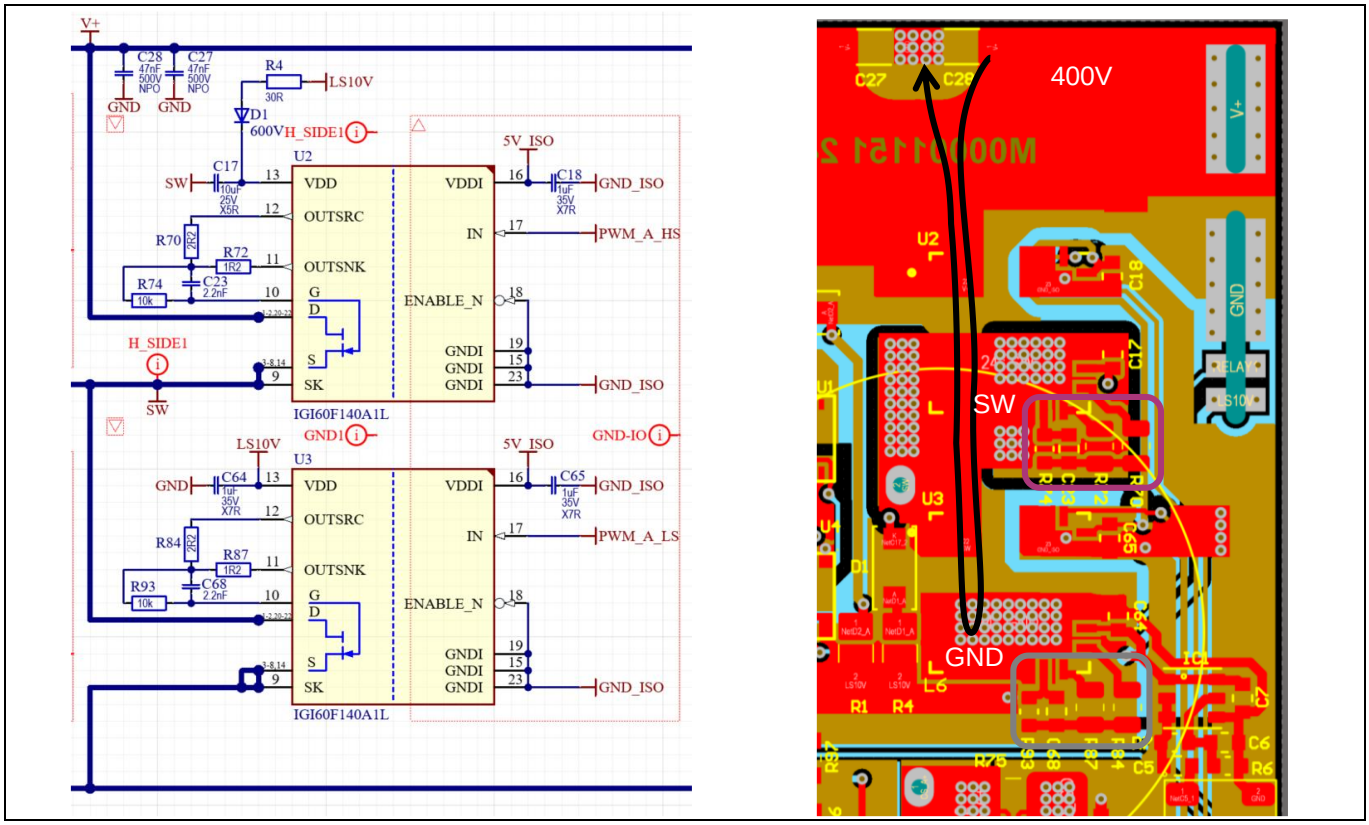


Figure 31 **Schematic of the totem-pole PFC (left) and layout (right) of the CoolGaN™ IPS for REF_240W_TP_PFC_GAN**

The layout is of great importance to obtain the maximum performance from CoolGaN™ HEMTs while avoiding oscillations and unwanted feedback into the device [10]. In REF_240W_TP_PFC_GAN, all components are placed on the top side of the main board, which enables the addition of a heatsink attached with a thermal interface material (TIM) to the bottom of the PCB. The multilayer (4-layer) design enables implementing a return path of the commutation loop in the inner layers (black arrow in Figure 31), minimizing the loop inductance. Furthermore, this ground plane avoids the RC network of the high-side CoolGaN™ HEMT, which is shielded by the switching node (purple area in Figure 31). In the case of the RC interface for the low-side device, the ground floor is in charge of shielding (grey area in Figure 31).

3.2 Operation of CoolGaN™ HEMT using unipolar supply voltage and bootstrap

In the case of a first startup or a soft-start operation after the PFC is turned off due to abnormal conditions (voltage sag, LCDO, and UVP), the PFC will always start at a negative AC cycle (in respect to the control ground). The reason behind this strategy is the bootstrap circuit of the low-frequency half bridge. If the converter waits for the proper AC polarity, the low-side switch of the return path can be switched on first; the bootstrap capacitor will have the energy for the following AC half cycle. For the same reason, the low-frequency switches keep operation during an OVP event. Example waveforms of both conditions are shown in Figure 32.

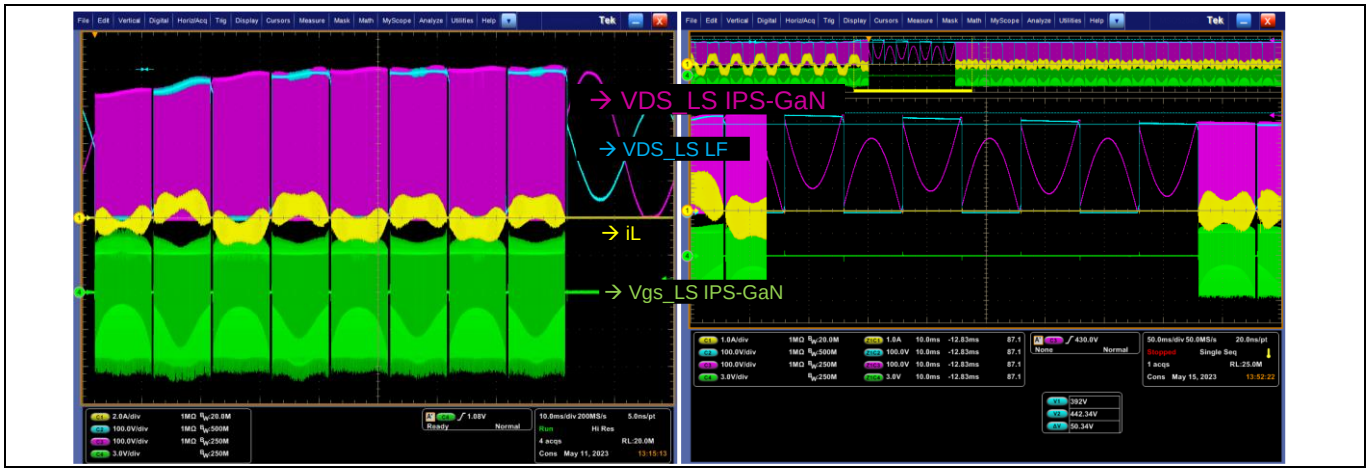


Figure 32 230 V startup begins at negative AC cycle (left) and low-frequency half bridge keeps switching during OVP event to ensure proper operation of the return path drivers bootstrap

On the operation of the high-frequency half-bridge, where a unipolar supply and bootstrap are being selected as supplying strategy for the high-side CoolGaN™ IPS, the microcontroller ensures that the high-frequency PWM always starts with the low-side switch. This enables the charging of the bootstrap capacitor to provide the following high-side switch pulse. In addition, it must be noted that a change in the switching node on either half bridge (low-frequency or high-frequency) when the PWM was disabled affects the other switching node through the input capacitor and inductor network. Given the low voltage threshold of CoolGaN™ devices and their low Cgd-Cgs ratio, a mis-trigger of the device could occur, and a shoot-through event could have fatal consequences for the converter, especially if negative voltage driving is not used such as in the case for the driving scheme used in REF_240W_TP_PFC_GAN.

With these considerations, it is important to understand the proper sequence between the low- and high-frequency half bridges to avoid commutation issues in CoolGaN™ devices. This sequence, which occurs after the PWM signals have been disabled at any condition, will be introduced in this section using the AC zero-crossing as an example, in which both the high- (HF) and low-frequency (LF) signals are momentarily disabled.

After a positive AC cycle in which the high-side (HS) switch of the LF half bridge was on, and the HS switch in the HF branch was acting as a boost switch, both switching nodes remain at a voltage close to the bulk voltage when the driving signals are disabled at AC zero crossing. In that case, starting the switching of the HF branch when the negative AC cycle starts would get the switching node to ground at a high dV/dt. Therefore, the HS drain-source voltage moves from almost ground to the bulk voltage with the same dV/dt with a potential risk of short-circuit through the Cgd-Cgs feedback.

Therefore, in this case, the LF half bridge is commutated first. By switching on the LS CoolMOS™ MOSFET in the LF half bridge, the switching node of the HF branch is moved to ground from almost the bulk voltage. It can be observed that this change in the switching node induces a change in the LS gate voltage (red arrow on Figure 33). An opposite reaction is expected in the high side gate-source voltage, which is not a problem in this case, but it could motivate a shoot-through if the LS gate source is also enabled as explained above. After the change in the LF half bridge, the controller waits for a defined time in which the switching node oscillates around the AC voltage. Afterward, the LS CoolGaN™ IPS starts operation as a boost switch (pink arrow). At this point, the Cgd capacitance has been considerably reduced, and the amount of charge is also significantly lower due to the reduced change in the drain-source voltage, virtually eliminating the possible gate feedback.

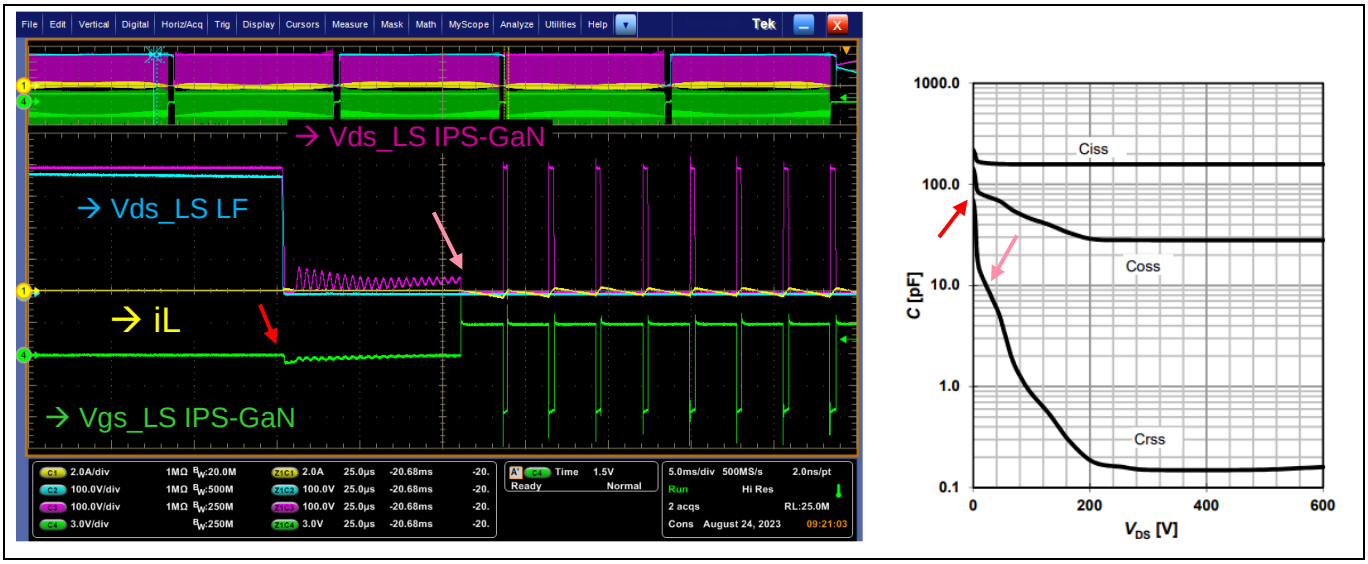


Figure 33 Applied sequence after AC crossing for negative AC cycle and capacitance variation as shown in the datasheet [12]

When considering the opposite transition for the AC voltage, both of the switching nodes are close to zero after the negative AC half-cycle, because the LS CoolMOS™ MOSFET was on and the LS of the HF half bridge was acting as a boost switch (long pulse for AC close to zero). Therefore, when the positive AC voltage cycle starts, the LS CoolGaN™ IPS can be switched on (red arrow on Figure 34) without triggering feedback in the HS device due to the very low voltage change. The switching of the HF branch forces the LF switching node to move from almost ground to the bulk voltage and the HS CoolMOS™ MOSFET can be triggered a defined number of switching cycles after this moment.

Because during the positive AC cycle (from the controller ground perspective), the LS transistor of the HF branch operates as the boost diode, a very short pulse would be applied during the first cycles due to the low AC voltage. As already mentioned, the HS switch is driven using a bootstrap capacitor and therefore, due to these very short pulses, the driver could potentially reach undervoltage lock out (UVLO). For that reason, the first pulse length is fixed to 2 µs in order to strengthen the supply voltage of the high-side driver.



Figure 34 Applied sequence after AC crossing for positive AC cycle

In the case of abnormal conditions, such as OVP or LCDO, the same principle explained above is applied. The main difference is that the time without PWM and/or low-frequency pulses is significantly higher: from some hundreds of microseconds in the case of AC crossing to 20 ms in LCDO or even more in the case of OVP. In these cases, it is possible that the UVLO of the HS drivers is triggered due to a voltage reduction on the bootstrap capacitor.

Figure 35 shows an example of discontinuous conduction mode (DCM) operation due to the lack of HS pulses for a few switching cycles when the PWM resumes after OVP (left). On the right side of the same figure, notice how the LF switching node is not clamped when the inductor currents get close to zero, which shows the lack of HS pulse for the LF half bridge after a 20 ms line cycle dropout at half load.

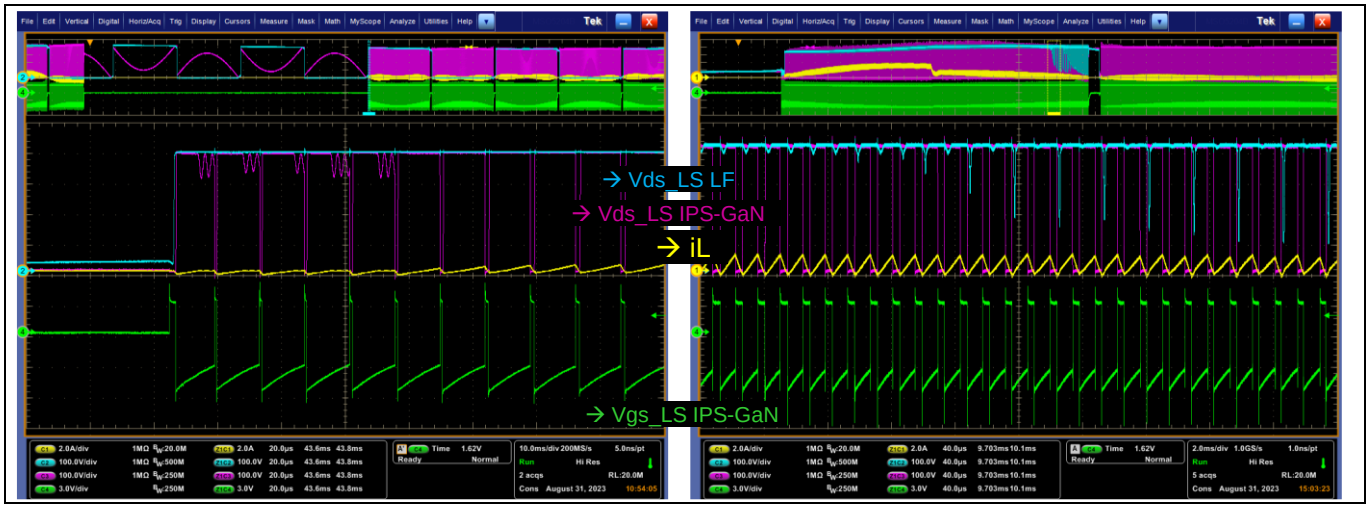


Figure 35 PWM resumes operation after OVP (left) and after 20 ms half-load LCDO at 315 degrees (right)

3.3 Variable dead-time for natural ZVS in partial load condition

In a classic boost PFC operating in CCM, there are two commutations every switching period at the on and off moments of the boost switch. When the boost switch is turned off, the inductor current flows naturally toward the bulk capacitor through the boost diode. However, when the transistor needs to turned on again, the current is hard-commutated from the diode to the switch. A totem-pole PFC operating in CCM is a synchronous boost PFC and the same commutations occur between two transistors. Figure 36 introduces the possible transitions in a synchronous boost converter in CCM at two different load points, which could be considered as a simplified totem-pole PFC for positive AC cycle.

On the left, Circuit A shows the boost switch (low-side LS switch)-to-boost diode (high-side HS switch) transition. As described above, in this transition, the current naturally flows to the output enabling the HS switch turning on with zero-voltage switching (ZVS). Because the time of this transition depends on the amount of current available in the PFC inductor (‘A’ points in the blue or green waveforms), the diode conduction time of the HS switch can be minimized by adapting the switch-to-diode dead-time in the PWM.

In high-load CCM where the current does not reach zero, the operation of synchronous boost is the same as for the classic boost; the current needs to be removed from the HS device when the LS switch is turning on (‘B’ in Figure 36). However, in a synchronous boost operation, the inductor current can be inverted at light load as shown by the green inductor current waveform. In this scenario, the reverse current during the HS (boost diode)-to-LS (boost switch) transition (‘C’ in Figure 36) enables ZVS turn-on for the LS switch. This kind of transition occurs at every switching cycle in the variable-frequency-operated triangular-current-mode PFC.

For a typical CCM totem-pole operation, the applied dead-time between the boost diode and boost switch is as short as possible to reduce diode conduction before the hard commutation occurs. Therefore, when the current reverts as shown in 'C', this dead-time needs to be prolonged to enable resonance between the inductor and the Coss capacitors of CoolGaN™ transistors.

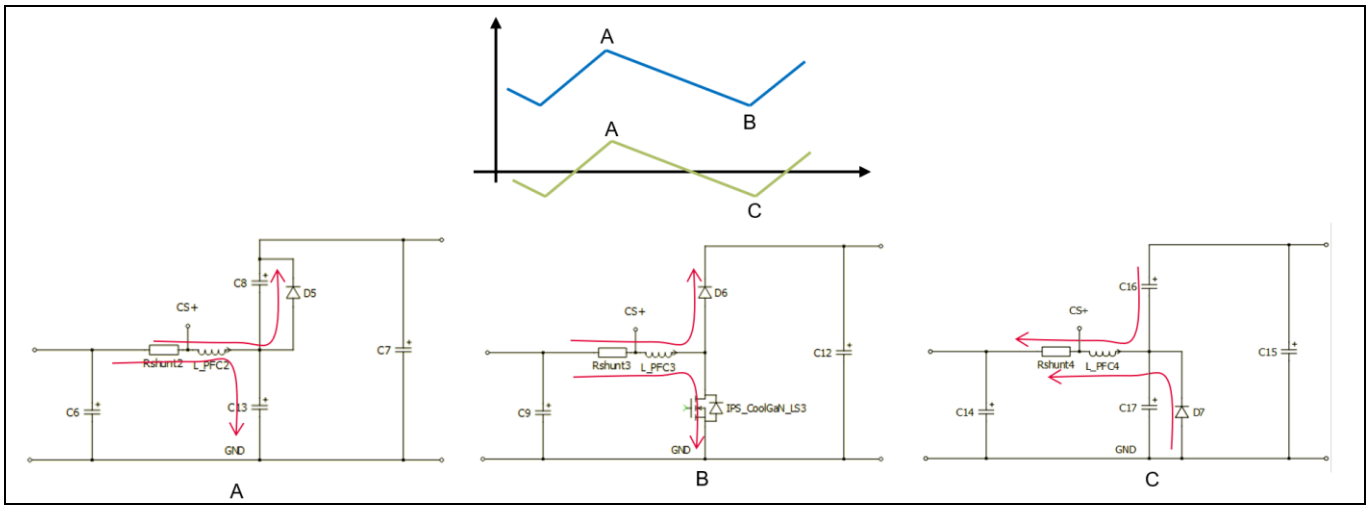


Figure 36 Inductor current for different load levels and possible commutation scenarios in a synchronous boost converter (placeholder)

In the case of a PFC operated in CCM, the average inductor current depends on the AC voltage and load conditions. Therefore, the peak and valley inductor current depend also on those parameters as well as the switching frequency, output voltage, and inductance value. Then, it can be calculated at which power the valley current is below zero for a given angle of the AC voltage. The blue curve in Figure 37.a presents this calculation considering that the valley current stays reversed for the whole AC cycle, which would enable ZVS operation for the AC cycle. In that case, ZVS is possible for power levels under 69 W at 100 V AC and under 82 W at 230 V AC. When the output power is under those values, a longer dead-time should be applied to the diode-to-switch transition to enable resonance while a short dead-time is applied for higher power levels to minimize the diode conduction time. In the selected implementation for REF_240W_TP_PFC_GAN, this dead-time is modified during AC zero crossing.

However, in high-line AC voltages, due to the lower current levels, it is easier to achieve the reverse current condition and prevent the degradation in performance due to diode conduction. This opens the possibility to increase the range of power levels in which a longer dead-time is applied by applying a longer dead-time until a power level in which the inductor valley current stays reversed for a percentage of the AC cycle, as shown by the red curve in Figure 37.a.

Figure 37.b shows the inductor average current (red) and peak (blue) and valley (green) envelopes for 230 V when the output power is 82 W (dashed lines), which corresponds to the condition in which the current changes polarity for the whole AC cycle, and for 186 W (solid lines), which corresponds to the scenario in which the current reverts during half of the AC cycle. This second condition is the one implemented in REF_240W_TP_PFC_GAN.

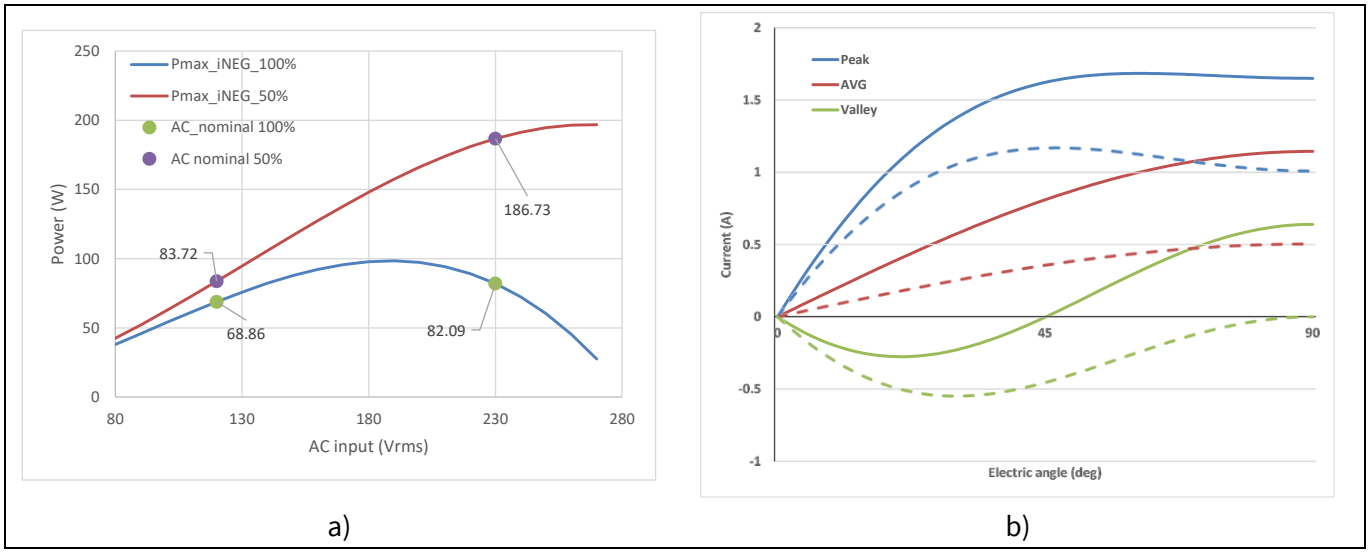


Figure 37 **a) Output power level to achieve reverse valley current during the whole AC cycle (blue) and during 50 percent of the AC cycle (red); b) Average, peak, and valley envelopes of the inductor current for 230 V and the load conditions specified on a).**

Switching waveforms are shown in Figure 38 to support this explanation. In this case, the inductor current and low-side CoolGaN™ IPS voltages are introduced for a similar angle in the AC with 140 W output power. On the left, at 230 V, it is clear that by applying a longer dead-time during the diode-to-switch transition, it is possible to obtain ZVS operation due to the reversed inductor current. On the right, however, because the current is not reverting for the same output power level and 100 V operation, a short dead-time is used to minimize the diode conduction time of CoolGaN™ IPS.

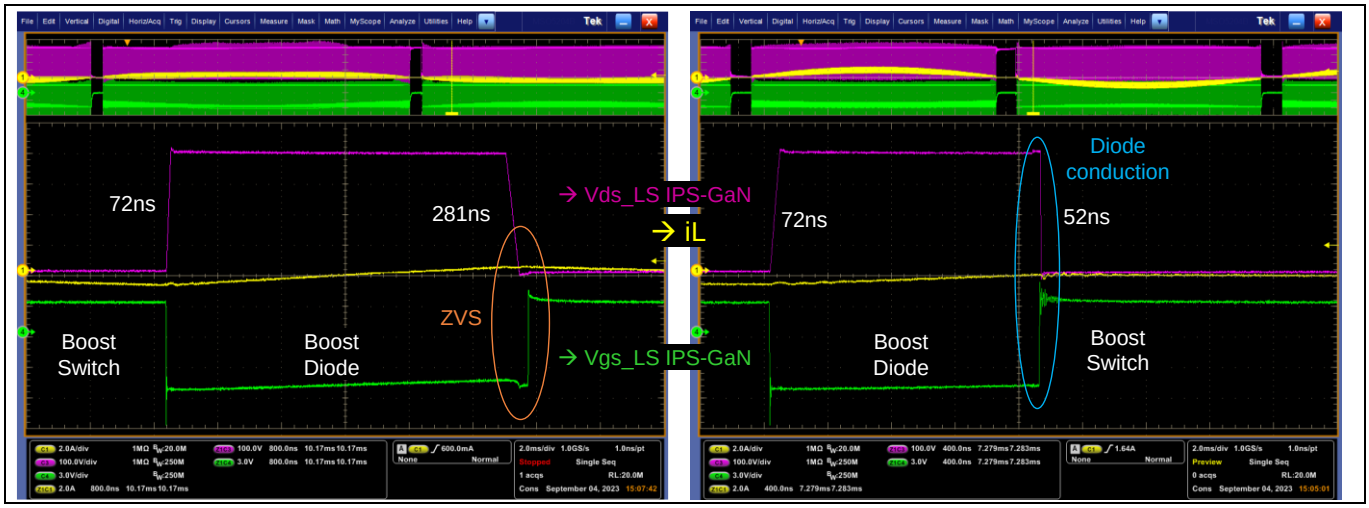


Figure 38 **Switching waveforms for 140 W operation and 230 V (left) and 100 V (right) at a similar AC angle**

The change in efficiency by applying this variable dead-time to enable ZVS operation when the current is reversed is shown in Figure 39. The measured efficiency when applying this strategy is shown in solid lines. The dashed lines show the measured efficiency when a short dead-time is applied as in the classical control approach.

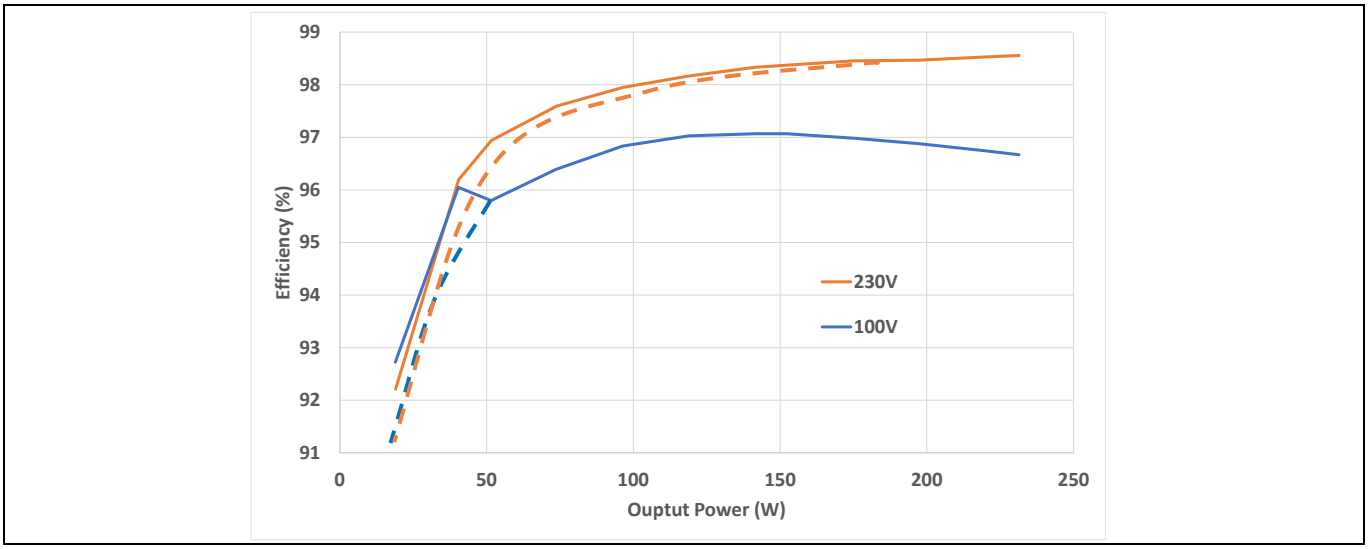


Figure 39 Efficiency variation with load when the diode-to-switch dead-time is modified according to the output power (solid lines) or it is kept constant (dashed)

3.4 Cooling system for final form factor and extended power range operation

As shown in Section 2.1.1, the thermal measurements were taken with the PFC choke outside of its final location. However, when the inductor is mounted in its corresponding place, thermal interaction between the devices in the main board and the PFC choke is expected. Figure 40 shows a long run test of a completely assembled REF_240W_TP_PFC_GAN in nominal operating conditions. The test was run with no added cooling system: no external fan or heatsink is attached.

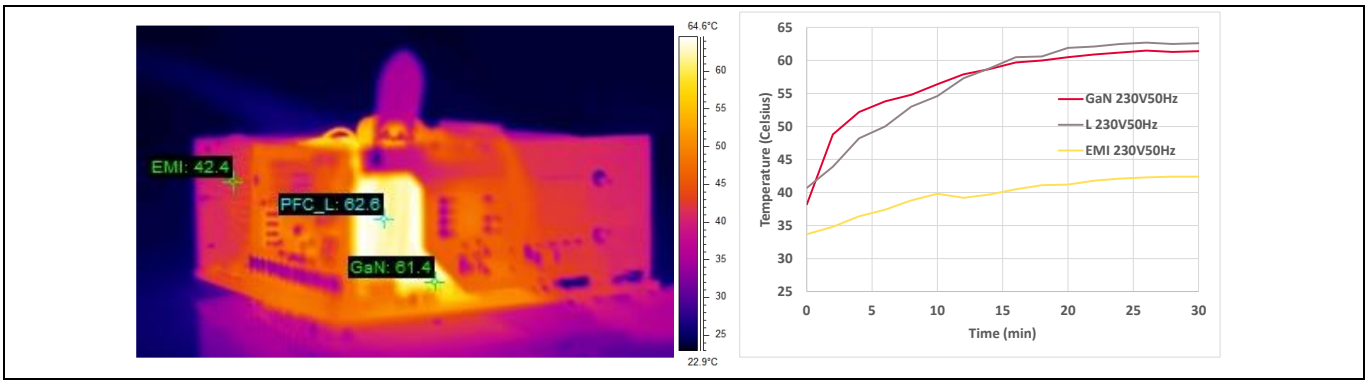


Figure 40 Thermal capture (left) after 30 minutes operation in nominal conditions and time evolution of temperatures during the test (right)

When the PFC operates at low line and full output power, a cooling system (or power derating) is required to limit the temperature rise of the CoolGaN™ IPS and CoolMOS™ devices in the main board. In such cases, a heatsink can be attached with the corresponding thermal interface material to the bottom of the main board. This bottom part has been left with no components, foreseeing the necessity of a cooling concept for the final application.

With such a cooling concept implemented in REF_240W_TP_PFC_GAN and provided that the reference board can operate up to 240 W at 120 V, the power range could be extended in high-line operation by keeping the input current under 2.1 A. That test has been run in an open board for 10 minutes (in the same conditions as described in Section 2.1.1) to explore the capability of extending the power range for high line, as shown in Figure 41. It can be seen that the temperatures reached are similar because the board is operating with the same input current.

Note: *REF_240W_TP_PFC_GAN firmware is prepared for 240 W operation to avoid larger currents at low line AC voltage. A firmware modification is therefore required to operate the board with extended power range at high line.*

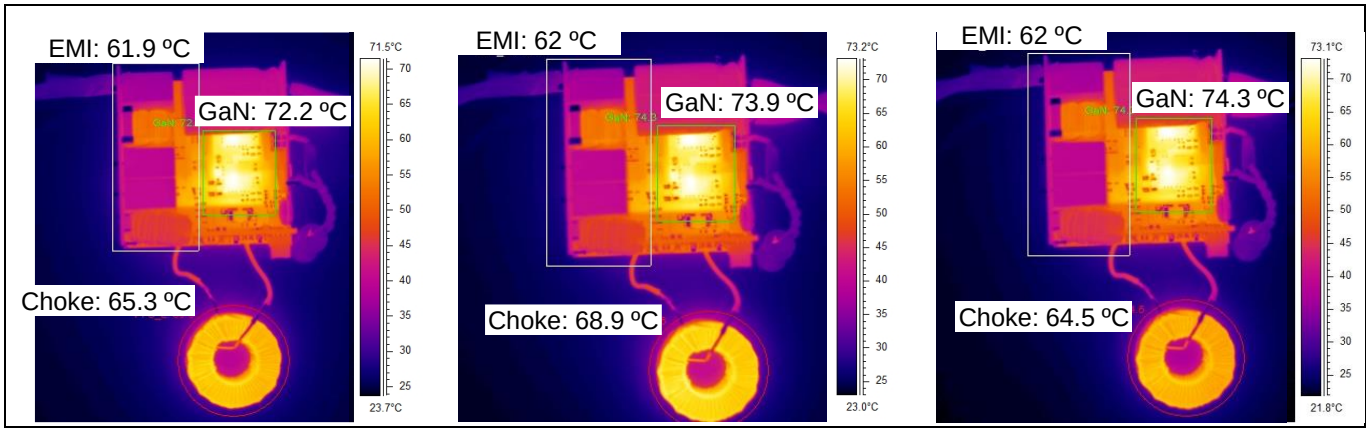


Figure 41 **Thermal captures after 10 min operation for 120 V – 240 W (left), 176 V – 360 W (middle) and 230 V – 480 W (right)**

Figure 42 and Figure 43 show the performance of REF_240W_TP_PFC_GAN for the extended power range at high-line AC voltage (maximum input current of 2.1 A), which correspond to the thermal captures shown above.

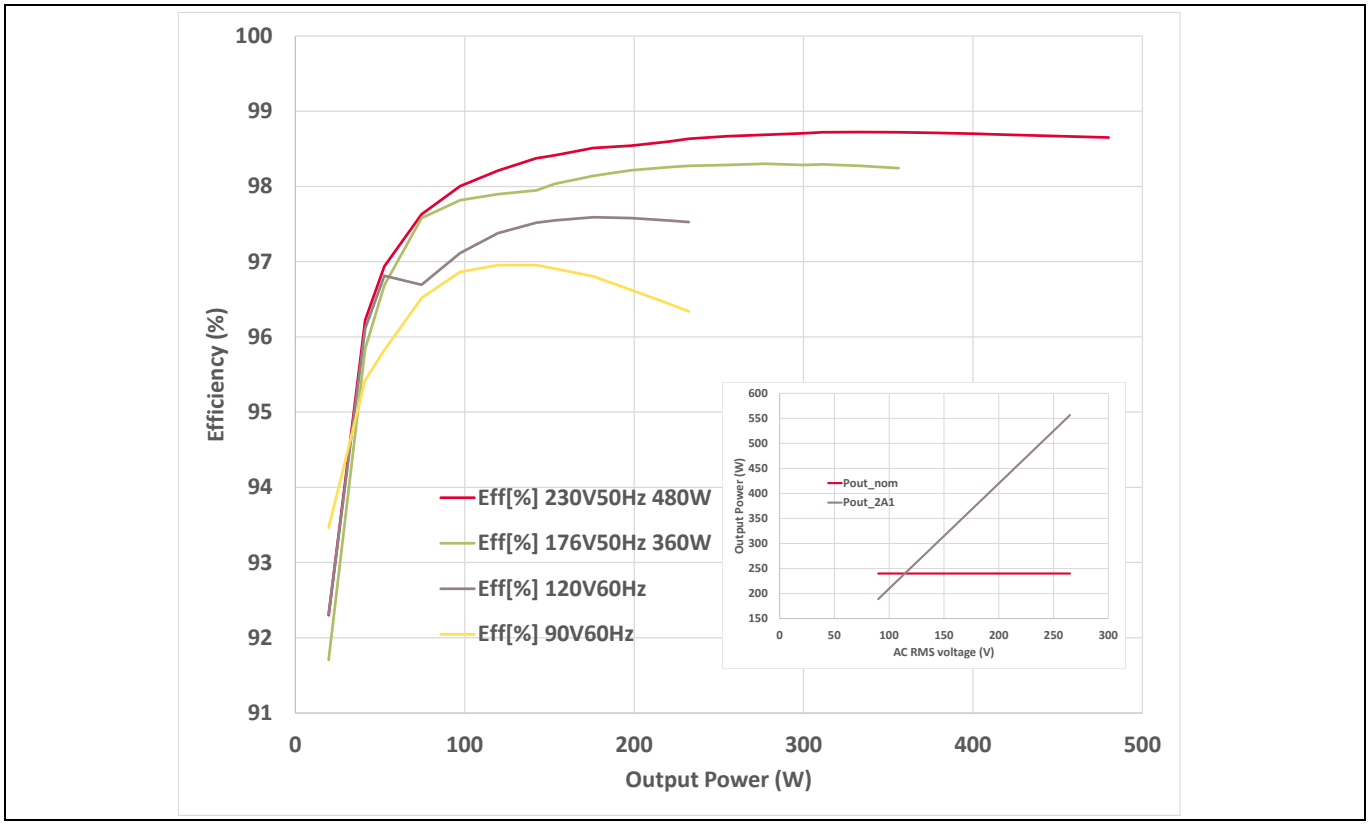


Figure 42 **Efficiency measurements for REF_240W_TP_PFC_GAN with extended power range and power variation according to AC line voltage and maximum input current of 2.1 A**

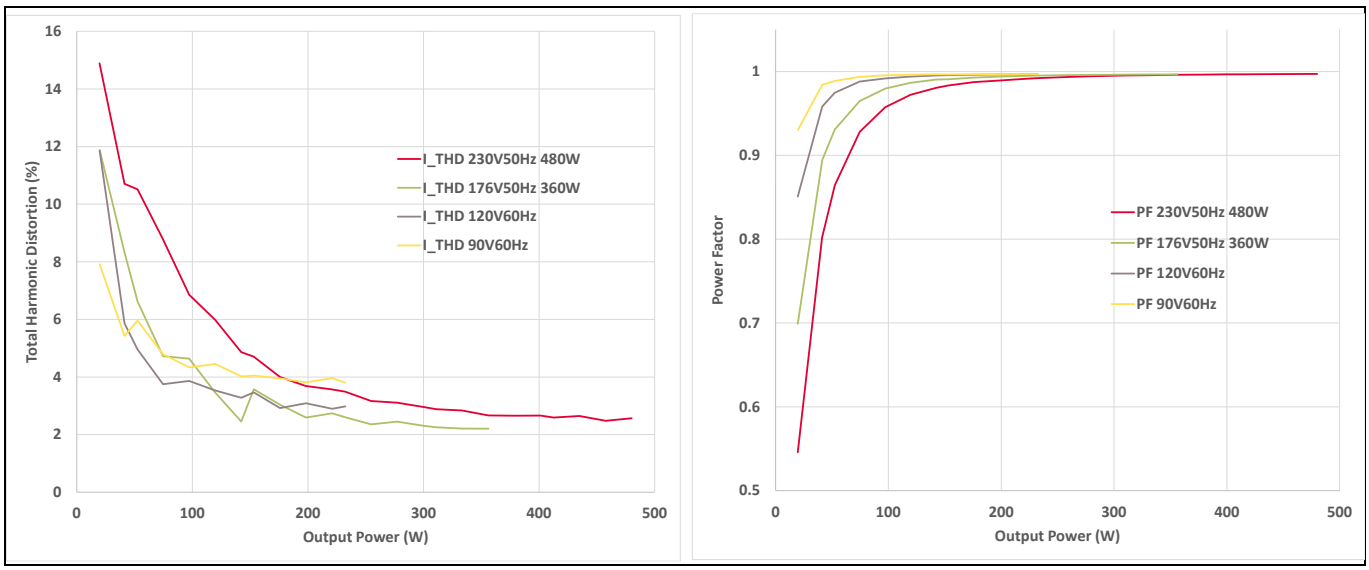


Figure 43 **THD (left) and power factor (right) measurements for REF_240W_TP_PFC_GAN with extended power range**

3.5 CrCM-TCM vs CCM EMI

For the power range targeted by REF_240W_TP_PFC_GAN, typically critical conduction mode (CrCM) is used because no current sensing is required and therefore both the cost and complexity of the solution are reduced. Furthermore, the advantage in performance can be achieved by taking advantage of the soft-switching or valley-switching operation. However, the variable switching frequency in the system, together with an eventual change in mode of operation between critical and discontinuous (DCM) conduction mode depending on the AC voltage and load conditions, considerably increase the design effort as well as the size of the EMI filter. On the other hand, if CCM is chosen as in REF_240W_TP_PFC_GAN, despite the hard-switching operation, the fixed-frequency operation simplifies the EMI design.

This section compares a differential-mode EMI spectrum between both modes of operation. The EMI emissions have been modeled in MATLAB based on the inductor current ripple following the methodology described in [7] and including the input capacitor of the totem-pole PFC. The estimated attenuation obtained by the EMI emission model is used to design a two-stage differential-mode EMI filter with the aim of comparing both modes of operation.

3.5.1 Comparison of EMI emissions and required attenuation

As a first step, CCM and CrCM operation are compared from the perspectives of inductor current ripple, switching frequency, and EMI spectrum. Also, triangular current mode (TCM [11]) is included in the comparison because it could offer advantages in performance due to its capability of soft-switching operation in all the AC and load conditions.

A PFC operating in CCM is modulated at constant switching frequency with a duty cycle variation to obtain an input current proportional to the AC input voltage. As a result, and depending on the inductor, the inductor current has a certain current ripple at the switching frequency. Figure 44 shows the inductance variation with current of the considered core as well as the inductor current ripple for that inductance and a switching frequency of 70 kHz. As it can be noted, four different voltages are considered in the analysis.

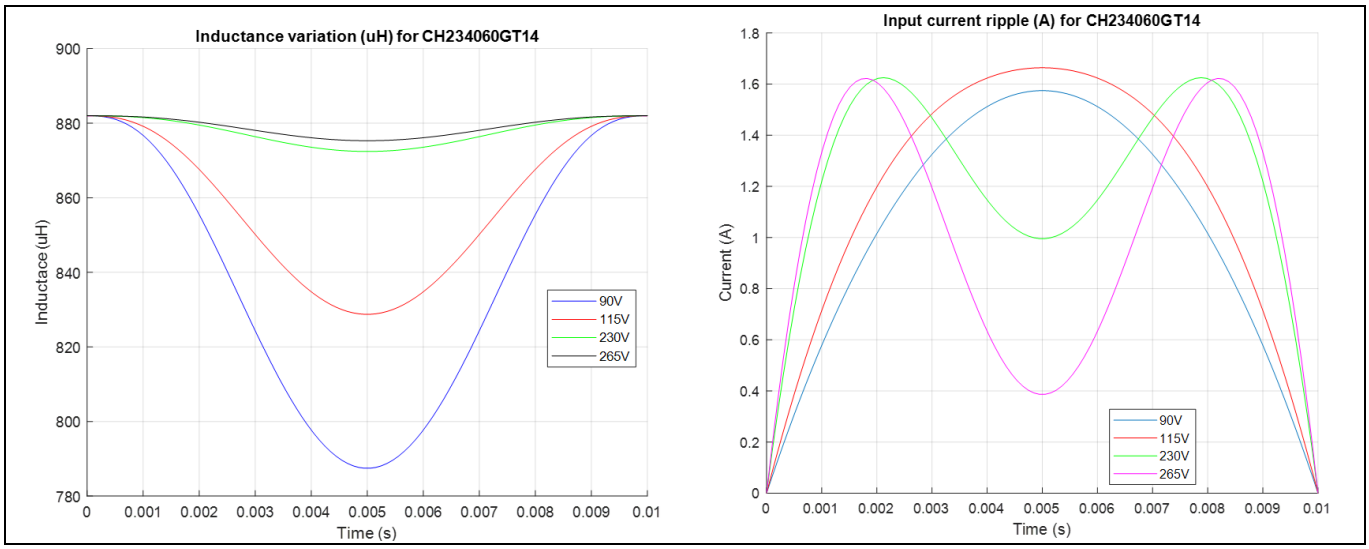


Figure 44 Inductance variation and inductor current ripple for REF_240W_TP_PFC_GAN at 70 kHz CCM operation

In the case of CrCM or TCM, the current ripple is given by the converter operation. In the case of CrCM, because the inductor valley current is set to zero, the peak current must be two times the desired average current. This restriction, together with the inductance value set in the design, determines the switching frequency. The same applies for TCM, but the peak envelope of the inductor current must consider the reversed current used to achieve full ZVS operation.

Because the switching frequency in REF_240W_TP_PFC_GAN is set to 70 kHz, two designs in CrCM and TCM with similar minimum switching frequency (72 kHz) at full load are selected for comparison. Figure 45 shows the current ripple and switching frequency for CrCM at full-load operation with a fixed inductance of 120 µH. As for CCM, four different AC voltages are considered in the analysis to cover the universal AC input range.

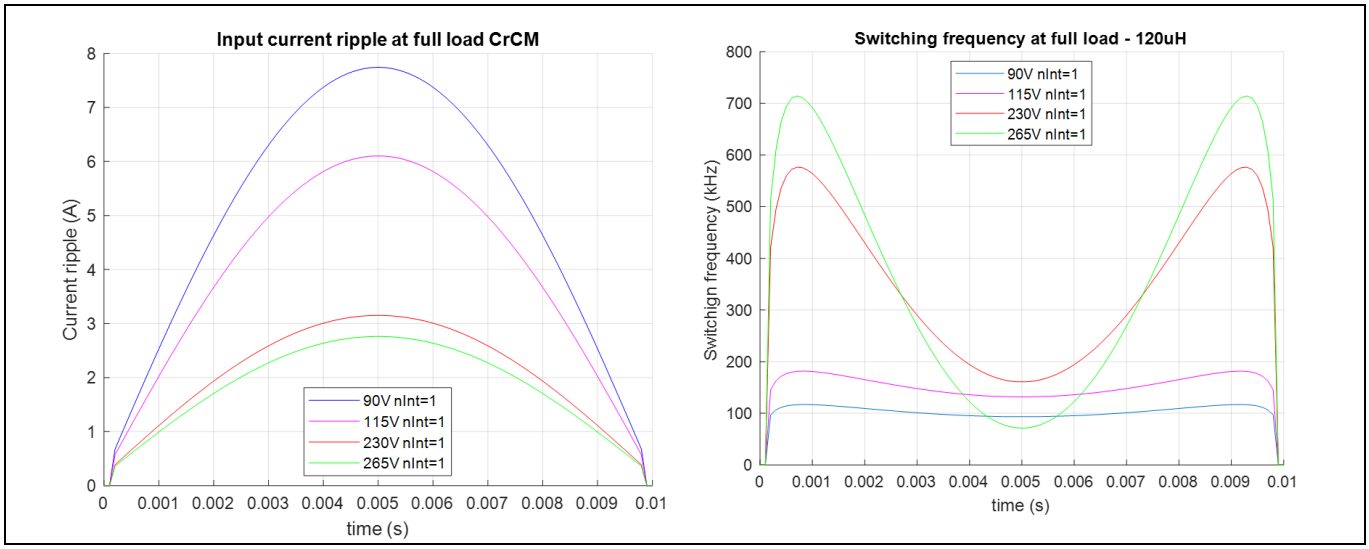


Figure 45 Inductor current ripple and switching frequency range at full load for a CrCM universal AC PFC with 120 µH inductor

In the case of TCM, because the current ripple is higher due to the reversed current to obtain soft switching, the switching frequency decreases with respect to CrCM. Therefore, the PFC inductance has been reduced to 60 µH to have similar minimum switching frequency as in CrCM and CCM as shown in Figure 46.

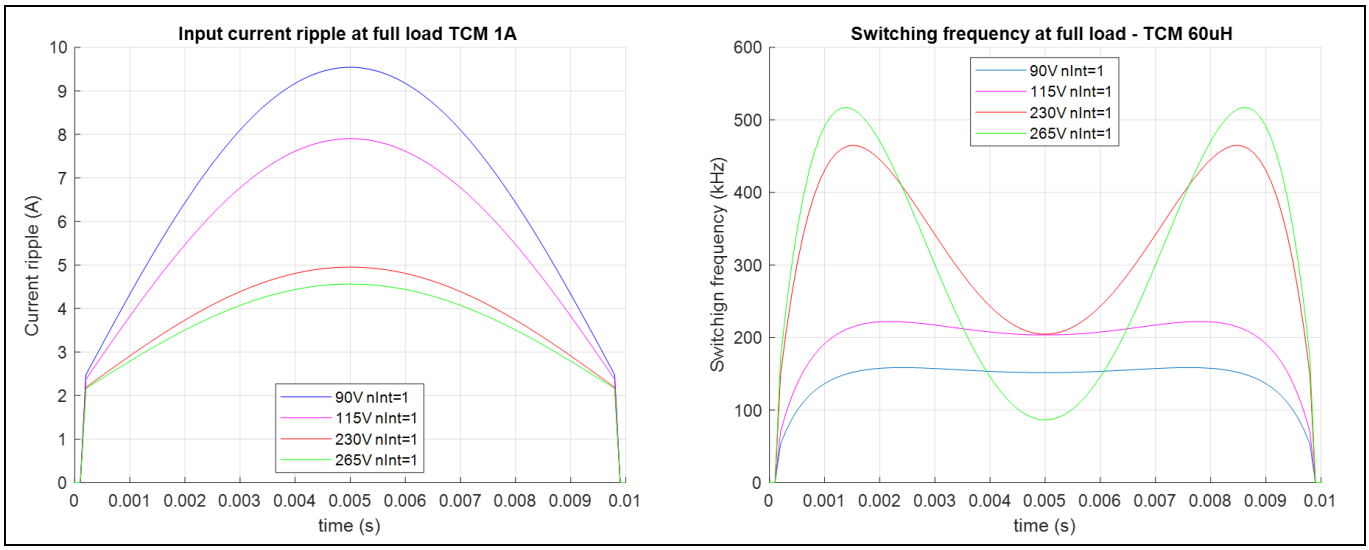


Figure 46 Inductor current ripple and switching frequency range at full load for a TCM universal AC PFC with 60 µH inductor and 1 A of reverted current for ZVS operation

The three designs shown above are then compared from their EMI emissions, as shown in Figure 47. It must be noted that the input capacitor of the totem-pole PFC is included in the calculations as an attenuation of the inductor current ripple. Due to the higher ripple in CrCM and TCM designs, a higher capacitance is in place for those designs: 820 nF in respect to 470 nF for CCM.

Even though the CCM design implements the lowest input capacitance in front of the PFC choke, based on the estimated differential mode EMI, it is obvious that CCM presents the lowest emissions at a higher frequency. In this case, the first harmonic in the spectrum corresponds to the third harmonic of the switching frequency (210 kHz).

According to the estimations, the CCM converter presented in this application note needs an attenuation of 48 dBµV at 210 kHz. In comparison, the CrCM design with 120 µH inductor would require 63 dBµV at 150 kHz and the TCM design with 60 µH estimation is 67 dBµV at 150 kHz. Therefore, it is possible to reduce the EMI for CCM operation with respect to a higher switching frequency design in CrCM or TCM, as shown in the following section.

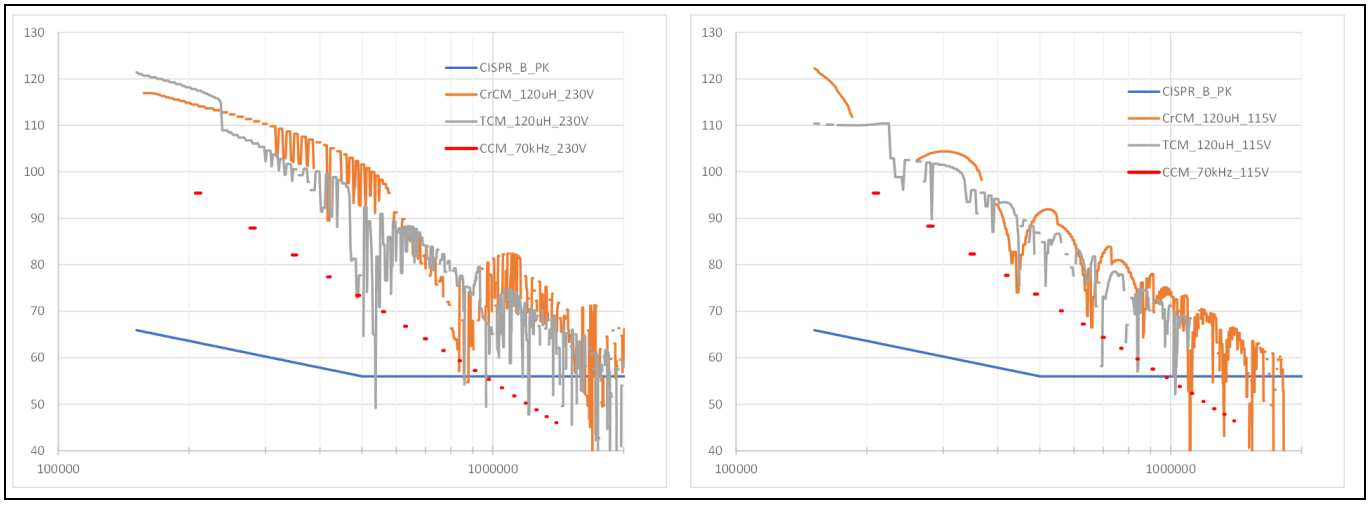


Figure 47 EMI spectrum comparison for 230 V (left) and 115 V (right) of CCM, CrCM, and TCM designs with similar minimum switching frequency (~70 kHz)

3.5.2 Differential mode EMI designs for CrCM, TCM, and CCM

Based on the estimation of required attenuation at the critical frequency obtained by modeling differential mode EMI emissions, the differential-mode EMI filter has been designed for the three considered operating modes.

In the case of 70 kHz CCM operation, the EMI filter design implemented in REF_240W_TP_PFC_GAN is shown in Figure 48. An asymmetric two-stage EMI filter is selected. The three X capacitors are 470 nF each. On the PFC side, a 90 µH differential mode choke is implemented while the grid side of the filter implements a common-mode choke with a stray inductance of 6 µH that provides differential mode filtering. A classical, and more conservative, approach is to design the filter with resonances at lower frequencies than the switching frequency. However, the asymmetric approach used in this design enables a size reduction with respect to the classic approach and allows achieving the required attenuation (dashed horizontal blue line) at the critical frequency (dashed horizontal orange line) and attenuates the switching frequency harmonic of the inductor current (vertical green line).

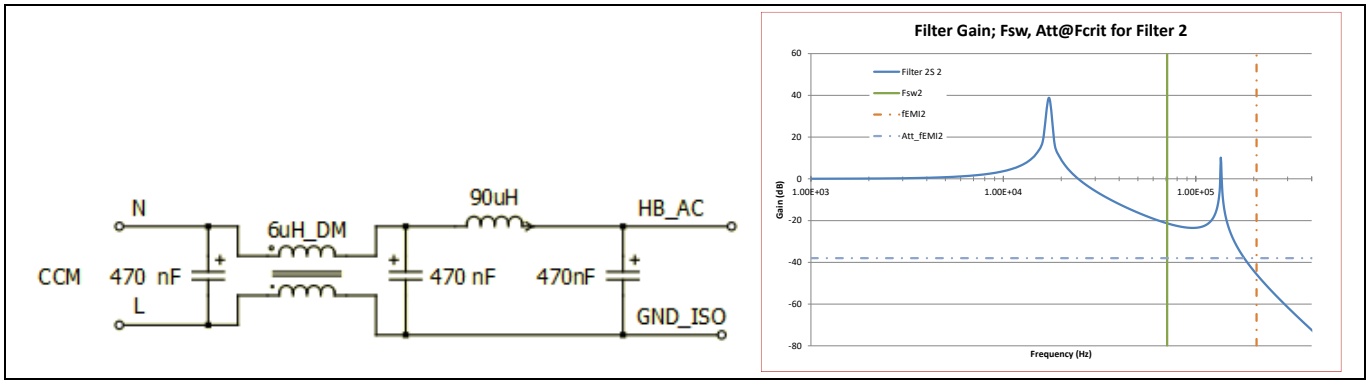


Figure 48 Differential-mode EMI filter design for CCM operation mounted in REF_240W_TP_PFC_GAN

For the CrCM and TCM designs, their differential-mode filter designs are presented respectively in Figure 49 and Figure 50. As already introduced, due to higher inductor ripple, the input capacitor in the totem-pole PFC is 820 nF instead of 470 nF. Furthermore, the other two X capacitors are 560 nF instead of 470 nF. This increased total capacitance has not only an adverse effect in size but also jeopardizes the achievable power factor.

To have a fair and intuitive comparison, the same asymmetric approach with the same common-mode choke on the AC side and the same 90 µH differential-mode choke in the totem-pole side implemented in the CCM filter are kept for these two designs. With that consideration, an extra differential-mode choke is required for both CrCM (54 µH) and TCM (44 µH). It must be noted that a different design approach for CrCM and TCM could be followed. However, note that the filter resonances must be at a lower frequency than the minimum predicted switching frequency (green vertical line) to avoid unwanted interactions and oscillations in the input current.

It can be then concluded that despite the possibility of increasing the switching frequency with a lower inductance (possible reduction of size of the inductor) offered by the soft-switching operation of CrCM and TCM, the power density for those designs is still significantly limited by the EMI filter design.

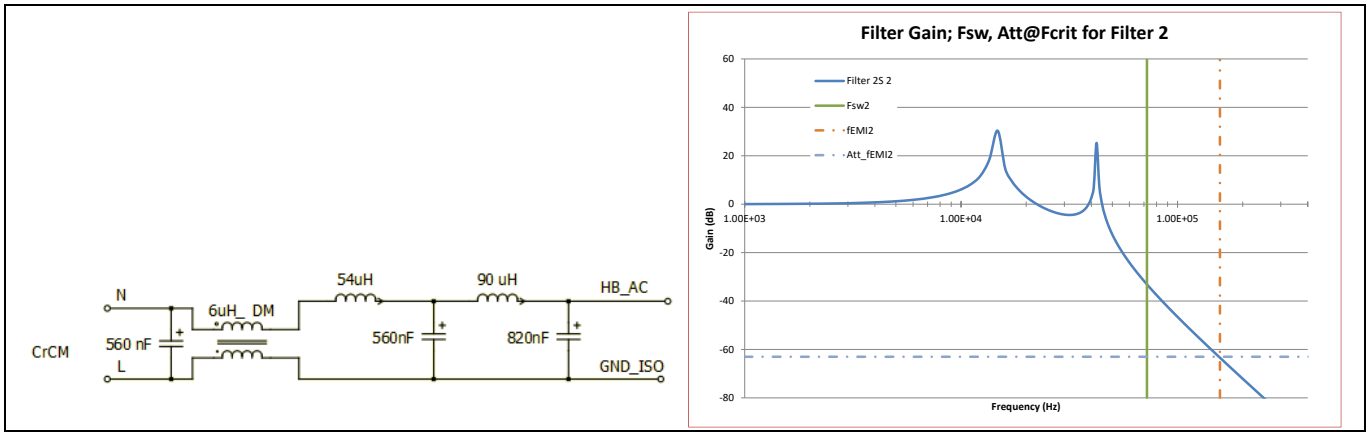


Figure 49 Differential-mode EMI filter design for CrCM operation of 240 W design with minimum switching frequency similar to those selected for CCM operation

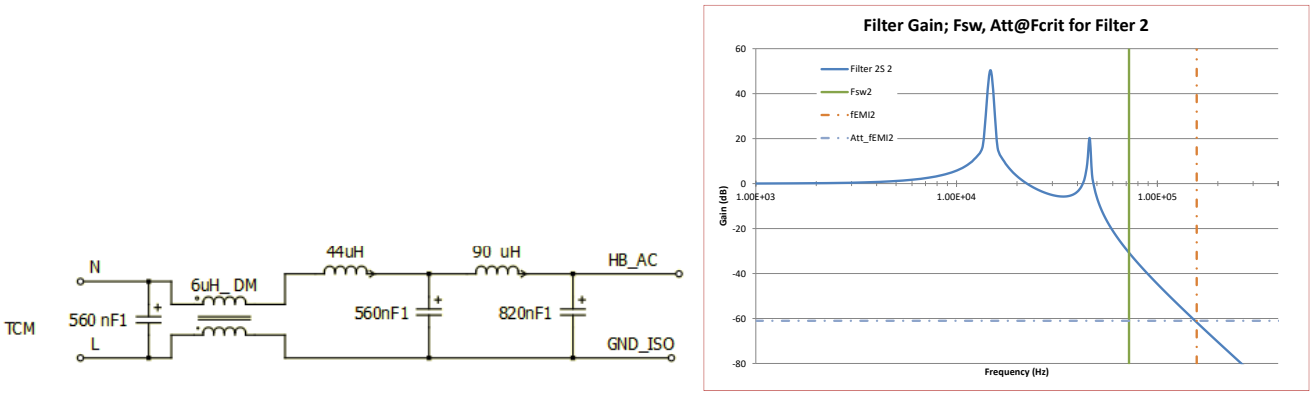


Figure 50 **Differential-mode EMI filter design for TCM operation of 240 W design with minimum switching frequency similar to those selected for CCM operation**

4 Summary

This document introduced an Infineon reference design for a low-power bridgeless totem-pole PFC operated in CCM targeting USB PD and battery charger applications. The reference board, which achieves a peak efficiency of 98.5 percent with a 20 mm low-profile form factor and a power density of 87 W/in^3, is enabled by using Infineon CoolGaN™ 600 V integrated power stage. The combination of the wide-bandgap switches and 600 V CoolMOS™ P7 MOSFETs allows high performance in a compact form factor, as described in this application note. The bridgeless topology implements full digital control on Infineon XMC™ 1000 series microcontroller.

The REF_240W_TP_PFC_GAN board has been tested using programmable AC source and electronic load to demonstrate not only the achievable high efficiency and the excellent input current quality (total harmonic distortion and power factor), but also the board capabilities in dynamic conditions such as load and AC voltage variations and abnormal operating conditions: voltage sag and line cycle dropout (hold-up time capability).

In addition, different design considerations are described in this application note. Recommendations for driving as well as indications on the layout requirements for CoolGaN™ IPS are provided in this document, together with further considerations for the operation of the GaN devices with a bootstrap concept. Because the totem-pole PFC described in this document operates as a synchronous boost converter and given the low power rate of the converter, there is possibility of realizing ZVS operation for some part of the converter operation. This document explores the conditions and necessary dead-time modifications for full soft-switching operation to occur.

Finally, a comparison with the most common operating mode for the power range of REF_240W_TP_PFC_GAN, i.e., critical conduction mode and its variation (triangular current mode) with the proposed continuous conduction mode is conducted for conducted differential-mode EMI estimation. The presented study shows how hard-switching CCM enables a smaller EMI filter than its soft-switching counterparts, despite the higher switching frequency achieved by those solutions.

5 Schematics

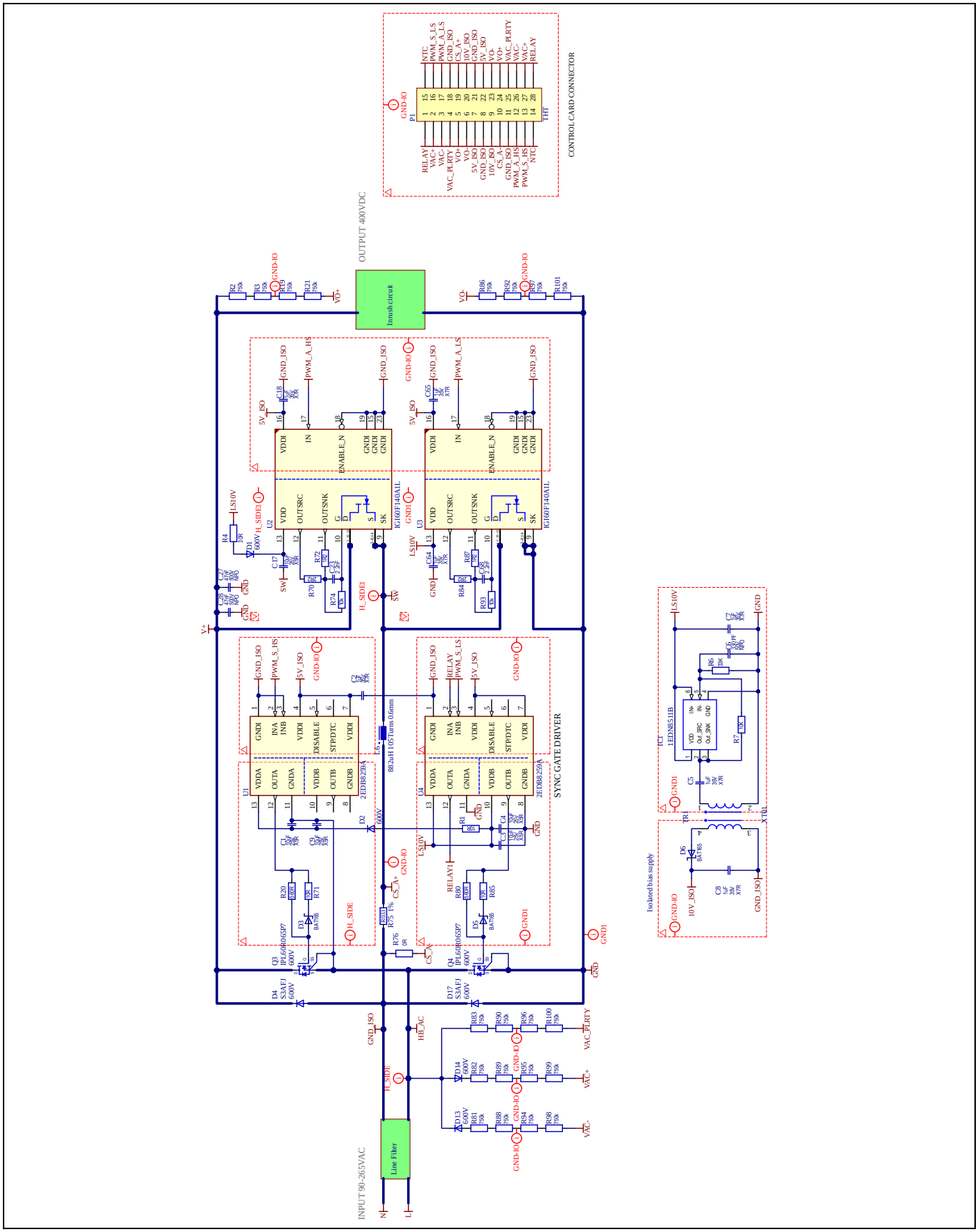


Figure 51 REF_240W_TP_PFC_GAN main board schematic

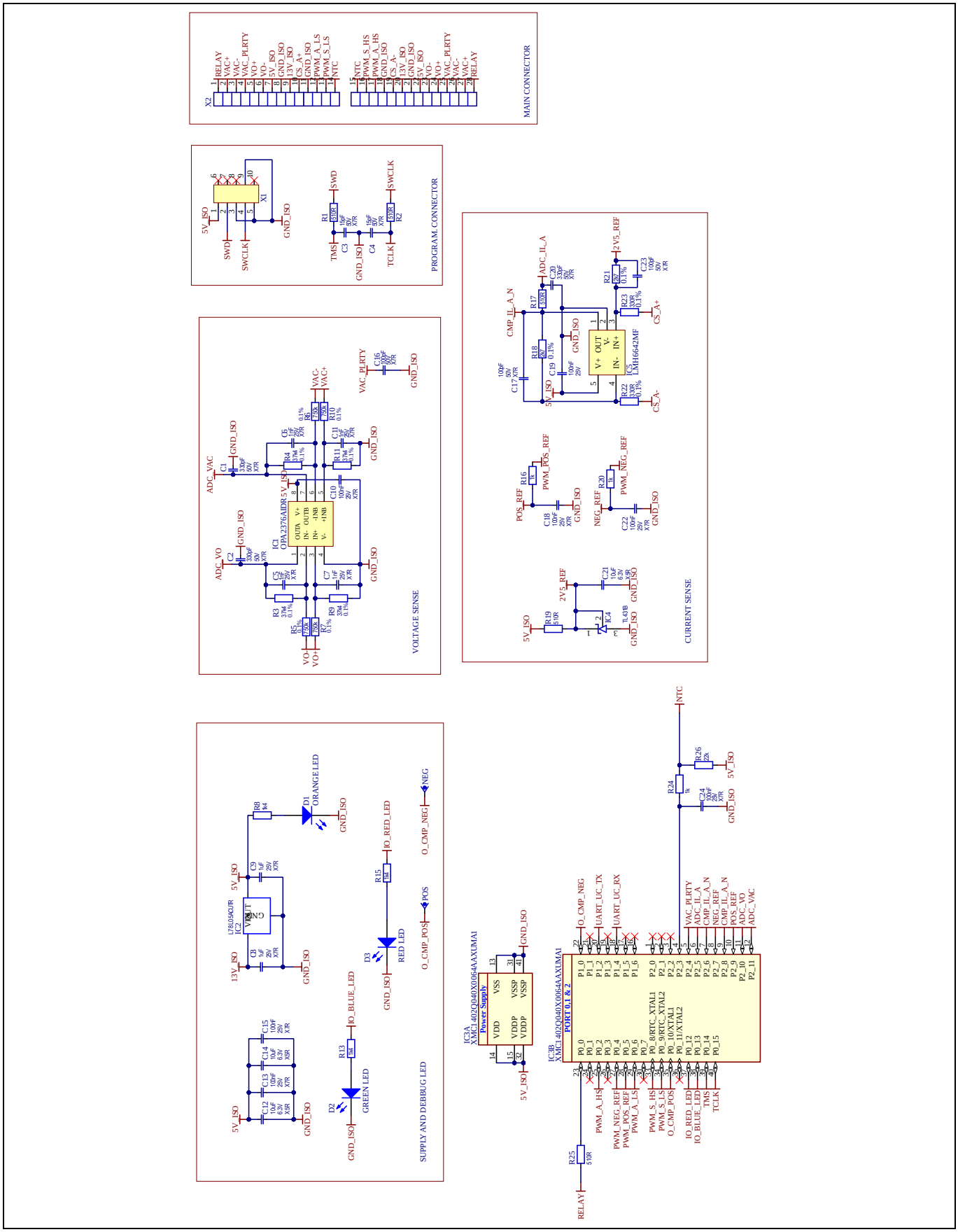


Figure 52 REF_240W_TP_PFC_GAN control card schematic

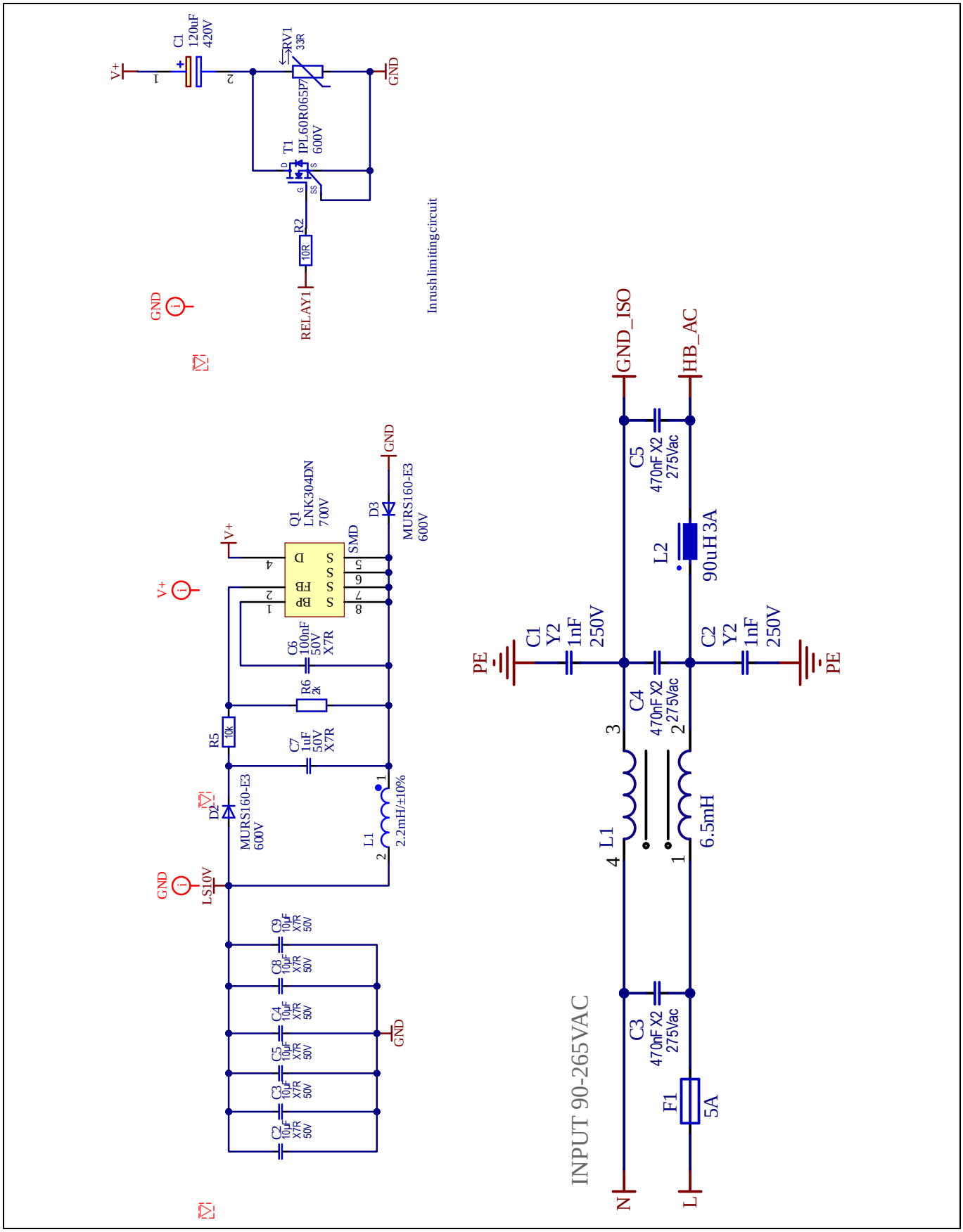


Figure 53 REF_240W_TP_PFC_GAN inrush capacitor and bias board (left) and EMI filter (right) schematic

6 Bill of materials

Table 6 Main board components in REF_240W_TP_PFC_GAN

Designator	Value	Tolerance	Voltage	Description
U2, U3	**IGI60F140A1L**	**–**	**600 V**	**600 V GaN power switch with isolated gate driver**
U1, U4	**2EDB8259A**	**–**	**–**	**Dual-channel isolated gate-driver IC**
Q3, Q4	**IPL60R065P7**	**–**	**600 V**	**N-MOSFET**
IC1	**1EDN8511B**	**–**	**–**	**Gate driver**
C1, C3, C4, C9	10 uF	X5R	25 V	Capacitor ceramic
C2, C5, C7, C8, C17, C18, C64, C65	1 uF	X7R	35 V	Capacitor ceramic
C6	330 PF	NPO	50 V	Capacitor ceramic
C23, C68	2.2 nF	X7R	50 V	Capacitor ceramic
C27, C28	47 nF	NPO	500 V	Capacitor ceramic
D1, D2	VS-1EFU06HM3/I	–	600 V	Standard diode
D3, D5, D6	BAT165	–	40 V	Schottky diode
D4, D17	S3AFJ	–	600 V	Standard diode
D13, D14	MURS160BT3G	–	600 V	Standard diode
L6	882 uH 105 Turns 0.6 mm	–	–	Inductor
R1	10 R	1%	–	Resistor
R2, R3, R19, R21, R81, R82, R83, R86, R88, R89, R90, R92, R94, R95, R96, R97, R98, R99, R100, R101	750k	0.10%	–	Resistor
R4	30 R	1%	–	Resistor
R6	33 K	1%	–	Resistor
R7, R74, R93	10 K	1%	–	Resistor
R20, R80	560 R	1%	–	Resistor
R70, R84	2R2	1%	–	Resistor
R71, R85	10 R	1%	–	Resistor
R72, R87	1R2	1%	–	Resistor
R75	R033	1%	–	TLRP3A30DR033FTE
R76	0R	1%	–	Resistor
TR1	XT01	–	–	Transformer

Table 7 Control card components in REF_240W_TP_PFC_GAN

Designator	Value	Tolerance	Voltage	Description
IC3	XMC1402Q040X0064AAXUMA1	–	–	Microcontroller
C1, C2, C20	330 pF	X7R	50 V	Capacitor ceramic
C3, C4	15 pF	X7R	50 V	Capacitor ceramic
C5, C6, C7, C11	1 nF	X7R	25 V	Capacitor ceramic
C8, C9	1 uF	X7R	25 V	Capacitor ceramic
C10, C13, C15, C18, C19, C22, C24	100 nF	X7R	25 V	Capacitor ceramic
C12, C14, C21	10 uF	X5R	6.3 V	Capacitor ceramic
C16, C17, C23	100 pF	X7R	50 V	Capacitor ceramic
D1	ORANGE LED	–	–	LED
D2	GREEN LED	–	–	LED
D3	RED LED	–	–	LED
IC1	OPA2376AIDR	–	–	Integrated circuit
IC2	L78L05ACUTR	–	–	Integrated circuit
IC4	TL431B	0.50%	–	Integrated circuit
IC5	LMH6642MF	–	–	Integrated circuit
R1, R2, R17, R19, R25	510R	1%	–	Resistor
R3, R4, R9, R11	37k4	0.10%	–	Resistor
R5, R6, R7, R10	750k	0.10%	–	Resistor
R8, R13, R15	1k4	1%	–	Resistor
R16, R20, R24	1k	1%	–	Resistor
R18, R21	2k7	0.10%	–	Resistor
R22, R23	330R	0.10%	–	Resistor
R26	22k	1%	–	Resistor
X1	FTSH-105-01-L-DV-K	–	–	Connector
X2	–	–	–	Pin header 2x14 contacts

Table 8 Bias and bulk capacitor board components in REF_240W_TP_PFC_GAN

Designator	Value	Tolerance	Voltage	Description
T1	IPL60R065P7	–	600 V	NMOSFET with Source Sense
C1	120 uF	–	420 V	Capacitor Polarized
C2, C3, C4, C5, C8, C9	10 uF	–	50 V	Capacitor ceramic
C6	100 nF	X7R	50 V	Capacitor ceramic
C7	1 uF	X7R	50 V	Capacitor ceramic
D2, D3	MURS160-E3	–	600 V	Standard diode
L1	2.2 uH	±10%	–	WE-TI radial leaded wire-wound inductor
Q1	LNK304DN		700 V	Buck controller
R2	10R	1%	–	Resistor
R5	10k	–	–	Resistor
R6	2k	–	–	Resistor
RV1	33R	±20%	–	NTC resistor

Table 9 EMI filter board components in REF_240W_TP_PFC_GAN

Designator	Value	Tolerance	Voltage	Description
C1, C2	1 nF	Y2	250 V	CAS17C222MARGC
C3, C4, C5	470nF X2	10%	275 Vac	Capacitor foil
F1	5 A	–	–	Fuse
L1	6.5 mH	–	–	Common-mode choke inductor
L2	90 uH 3 A	–	–	Differential-mode inductor

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